Is there an automated way to address and select local scan ports of the TF112 ?

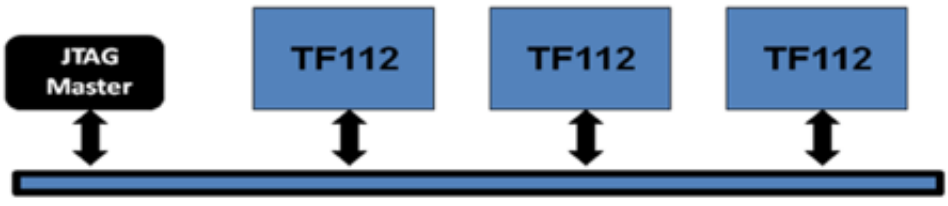
Auto-Test-Pattern-Generation (ATPG) from all of the leading vendors (Asset, Goepel, JTAG Technologies) include addressing and LSP selection algorithms for the TF112. The software supports testing using a single LSP, interconnect test involving multiple LSPs and even interconnect testing involving LSPs on 2 different TF112s. An example is JTAG Technologies … http://www.jtag.com/

How can I accelerate programming times when using a TF112?

Devices to be programmed should be placed on as short a chain as possible. Higher TCK speeds can generally be achieved when the TF112 is in “Bridge Mode” as opposed to “Transparent”. When programming Flash, a R/W* toggle signal such as generated by JTAG Technologies auto-write …… (add link) . The TF112 includes pass-thru bits for buffering this type of signal.

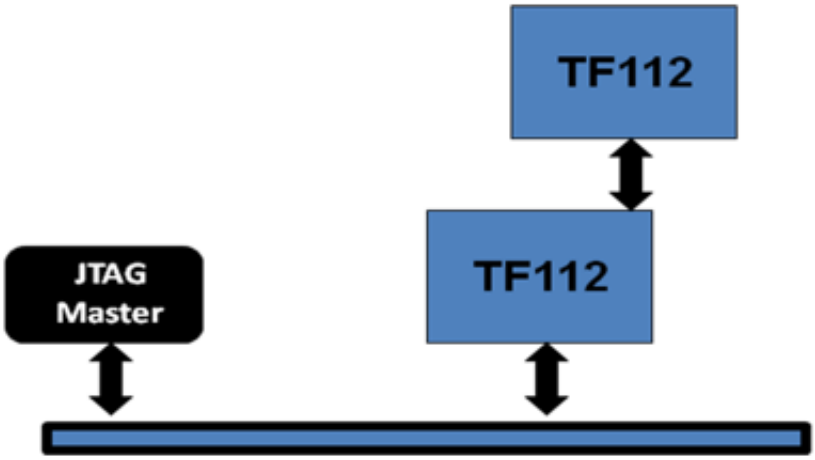
Since TF112s can support multi-drop or be cascaded (hierarchical), what is the preferred architecture ?

Although both multi-drop and a hierarchical scan tree are supported in hardware, the multidrop approach is simpler for ATPG (Auto-Test-Pattern-Generation) software and in general is the preferred architecture.



TF112 in Multi-drop Architecture

TF112 in Multi-drop Architecture



TF112 in Multi-drop Architecture

How do I handle non-compliant IEEE1149.1 devices where TRST* must remain in the HIGH state ?

Devices that require TRST* to remain HIGH can be accommodated using the TLR_TRST pin. When asserted this pin forces the selected LSP to keep TRST HIGH.

Is the TF112 compatible with the National Semiconductor STA112?

The TF112 is a direct drop-in replacement for the SCANSTA112. The ID code register has the same base ID only the version and vendor portion has changed. In addition the TF112 has the added feature of register access to the pass-through bits.

Is it necessary to address and configure the TF112 through the backplane port?

Configuration can be accomplished either via scan instructions loaded through the backplane port or utilizing the external Sx (select LSP) pins.

I have used 1149.1 (JTAG) for some time now, when is a good time to start considering system test devices such as the TF112?

As systems increase in complexity the advantages of multiple scan chains become apparent. Some examples where system JTAG devices are typically used are as follows: 1) In systems with a backplane where cards may or may not be populated. Utilizing the addressable feature of the TF112 allows the user to target the cards that are present. 2) In systems where there are daughter cards that may or may not be populated. The ability to link in only the needed Local Scan Ports (LSPs) will allow the user to target the cards that are present in the system. 3) On complex cards with many high pin count digital devices. For best performance, ATPG vendors recommend a maximum of 5 to 7 devices on a chain. Additional devices create excessive electrical loading on the parallel signals TCK, TMS, and TRST requiring buffers and often slower TCK speeds. Multiple chains reduce test, debug and programming times.
