TELEFUNKEN
Semiconductors

USER MANUAL

400 Mbps Quad LVDS Line Receivers with Extended Common Mode TF90LVDS047-048 Evaluation Board

Features

- **TF90LVDS048's wide common mode input range, from -7V to +12V.**
- **Separate Power and Ground Planes for Each Device.**
- **Three Types of Interconnections**
  - **Channels #1 and #2 CAT5 (RJ-45)**
  - **Channel #3 Microstrip**
  - **Channel #4 Ribbon Cable Header**

Description

The TF90LVDS047_048EVK is an evaluation board designed to demonstrate all of the features and performance of the TF90LVDS047 and the TF90LVDS048.

These devices are a 400 Mbps Quad LVDS (Low Voltage Differential Signaling) Line Driver and Receiver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e.g. cables, printed circuit board traces, backplanes). Its flow-through pinout simplifies PCB layout and minimizes crosstalk by isolating the LVDS outputs from the LVCMOS / LVTTL inputs

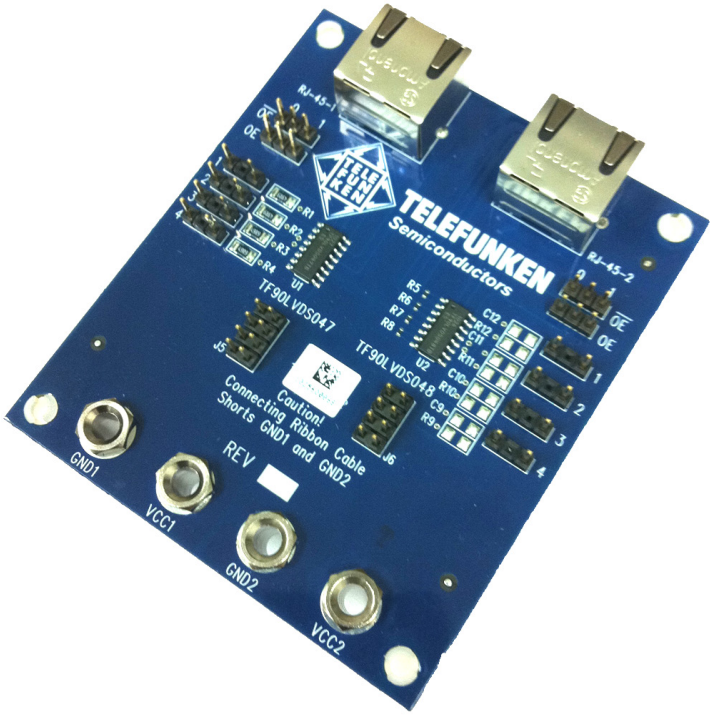
The TF90LVDS047 accepts four LVCMOS / LVTTL signals and translates them to four LVDS signals. Its differential outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

The TF90LVDS048 accepts four LVDS signals and translates them to four LVCMOS signals. Their outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*. There is also a TF90LVDT048 available with the same funtionality as the TF90LVDS048 but with an internal 100Ω termination resistor.

To demonstrate the TF90LVDS048's wide common mode input range, from -7V to +12V, each of the devices has its own isolated power and ground planes. This enables the user to apply an offset voltage between GND1 and GND2 emulating a system where the grounds are at different potentials. When connecting bench equipment to the offset grounds ***Caution*** should be exercised to avoid ground loops.

There are three types of interconnects provided to facilitate the user in evaluating the effects of various interconnect media on signal integrity. ***Caution*** should be used when connecting a ribbon cable to complete the connection between channel #4. This will short the two ground planes potentially leading to a ground loop.

Evaluation Board Photo



Ordering Information

PART NUMBER	MAIN IC (U1) PART NUMBER
TF90LVDS047_048EVK	TF90LVDS047-TBU
	TF90LVDS048-TBU

Applications

- Digital Copiers
- Wireless Base Stations
- Telecom / Datacom
- Network Routing
- Laser Printers
- LCD Displays

Overview

Channels #1, #2, and #3 of the evaluation board can be represented by the simplified schematic in Figure 1. Channel #4 has the ability to connect GND1 to GND2 through the ribbon cable and is not shown. The TF90LVDS047 on the left side is connected to VCC1 and GND1. The input port and return path for the 50Ω termination resistor are connected to GND1 as well. The TF90LVDS048 on the right side is connected to VCC2 and GND2. The output port is referenced to GND2.

Channels #1 and #2 interconnects are completed using a cat5 cable plugged into the RJ-45 jacks on the board. Each of the two channels is connect through a twisted pair in the cat5 cable, thus there is an approximate differential impedance of 100Ω. Channel #3 utilizes a microstrip trace with a 100Ω differential impedance on the top side of the board. Channel #4 is routed to an 8-pin headers that can be used with a ribbon cable or other types of interconnect media. Six of the eight pins of the header are connected to its local GND. If there is an offset between the two GND planes, connecting a ribbon cable will create a ground loop.

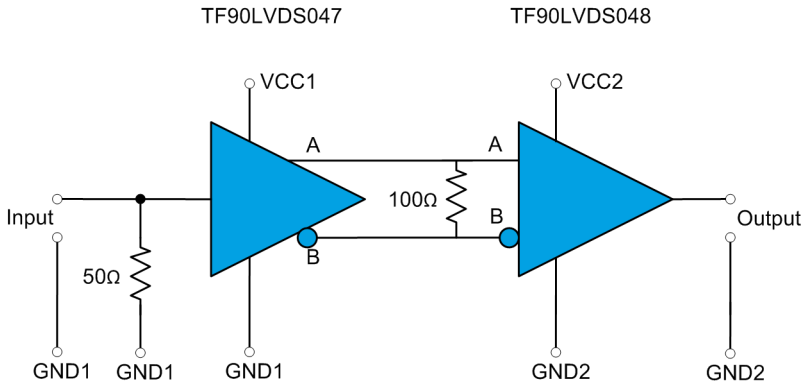


Figure 1. Simplified Schematic

Low Voltage Differential Signaling

There are two important advantages to the LVDS (Low Voltage Differential Signaling) approach to transmitting and receiving signals, first is that the receiver's input and transmitter's outputs do not share a current path. Second is that the input voltage is not referenced to ground but to the differential that is present between the two input pins of the receiver.

In the signal path between the two devices is a 100Ω termination resistor. From the output of the TF90LVDS047 there will be an appropriate amount of current flowing from its A terminal to its B terminal. This current is monitored by the output stage of the TF90LVDS047 such that the correct V_{OD} and V_{OS} are achieved. (See Figure 2) In the case of the TF90LVDS048 there is negligible current flowing from the termination resistor to the high impedance of its input, therefore, effectively isolating current paths between the two devices.

From the perspective of the receiver, the voltage generated across the 100Ω termination resistor is VID or the input differential voltage level. It is this voltage level that determines the logic level ('1' or '0') that the device is receiving. Typically, 100mV is sufficient to guarantee a valid signal. This voltage can also be referred to as VAB or the voltage at terminal A when referenced to terminal B, it is not VA or the voltage at terminal A when referenced to ground. When the VID and VOS are combined there is a resulting VA and VB and the LVDS standard limits these voltages from 0V to 2.4V whereas the TF90LVDS048's inputs are able to accept input voltage from -7V to +12V.

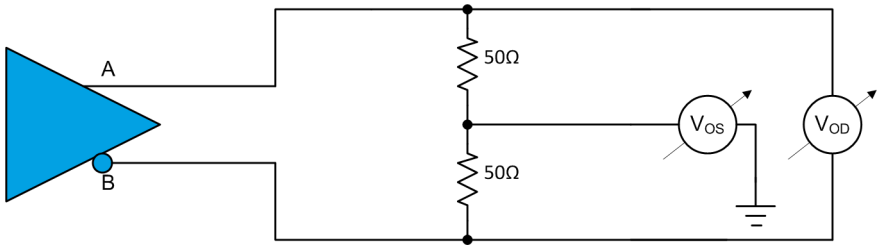


Figure 2. V_{OS} and V_{OS} measurements

0V Offset

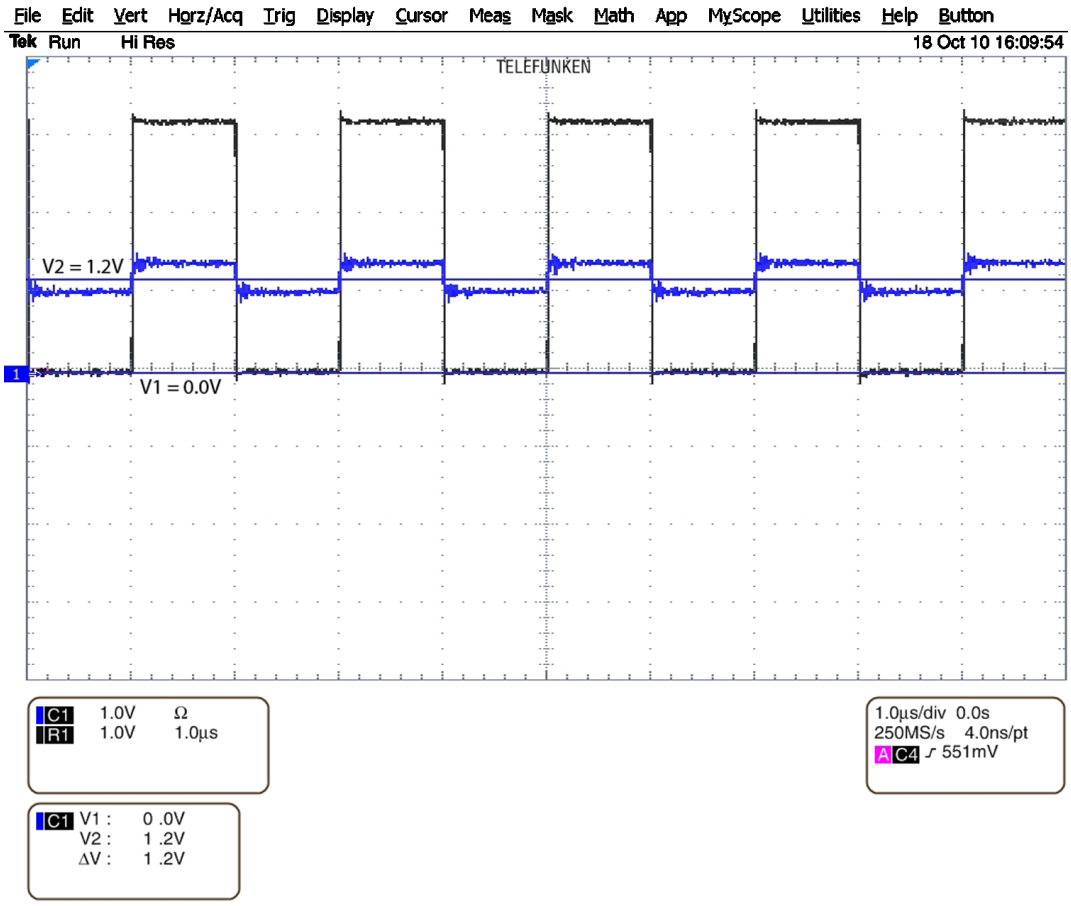


Figure 3. Scope plot at 0V Offset

Figure 3 is a scope plot where GND1 and GND2 are at the same voltage. The blue trace is V_A referenced to GND2 and the black trace is V_{output} referenced to GND2. Not shown is V_B which is an inverted version of V_A and is centered around 1.2V like V_A. As can been seen from the plot V_A reaches a maximum voltage of about 1.45V.

The V2 cursor is at 1.2V which is the V_{OS} of the TF90LVDS047.

Figure 4 is a schematic of the voltage supplies that are connected to the TF90LVDS047_048EVK. Noted that since $V_{SUPPLY}2$ = 0V GND1 and GND2 may be connected together.

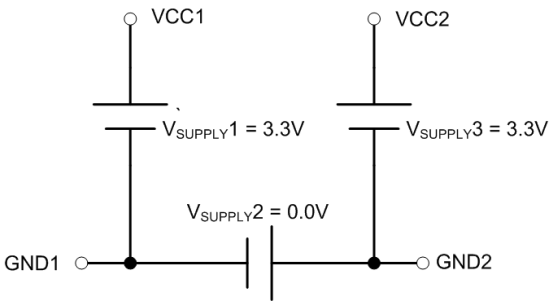


Figure 4. 0V Offset applied to the Transmitter

Positive 4V Offset

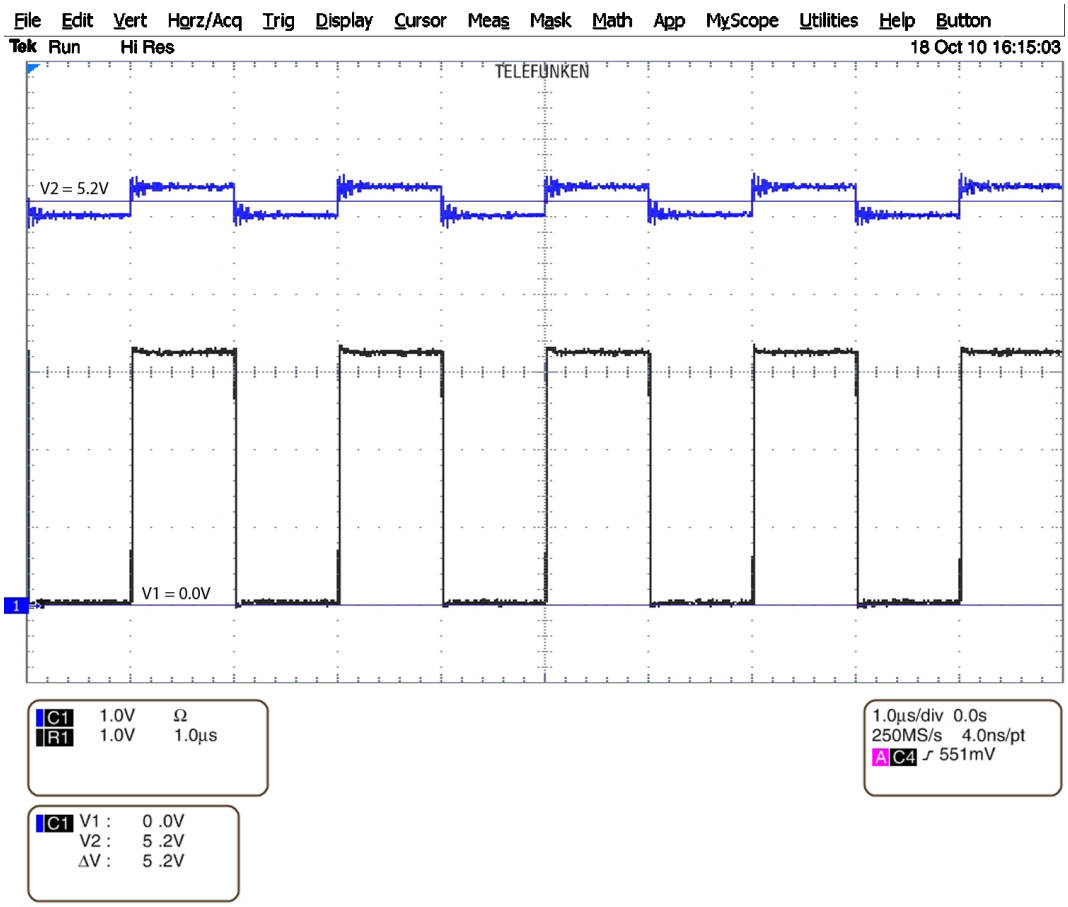


Figure 5. Scope plot at Positive 4V Offset

Figure 5 is a scope plot where GND1 is 4V greater than GND2 The blue trace is V_A referenced to GND2 and the black trace is V_{output} referenced to GND2. As can been seen from the plot V_A reaches a maximum voltage of about 5.35V, well outside of the LVDS allowable voltage but, because of the wide common mode range capability of the TF90LVDS048 this is an appropriate input.

The V2 cursor is at 5.2V which is the V_{OS} of the TF90LVDS047 plus the 4.0V applied offset voltage (1.2 + 4.0 = 5.2).

Figure 6 is a schematic of the voltage supplies that are connected to the TF90LVDS047_048EVK. Noted that since $V_{SUPPLY}2$ = 4.0V GND1 and GND2 may NOT be connected together.

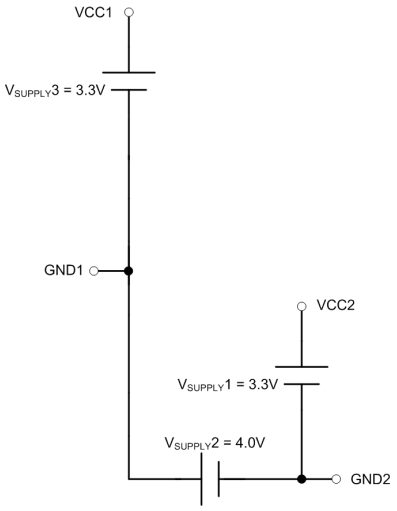


Figure 6. Positive 4V Offset applied to the Transmitter

Negative 4V Offset

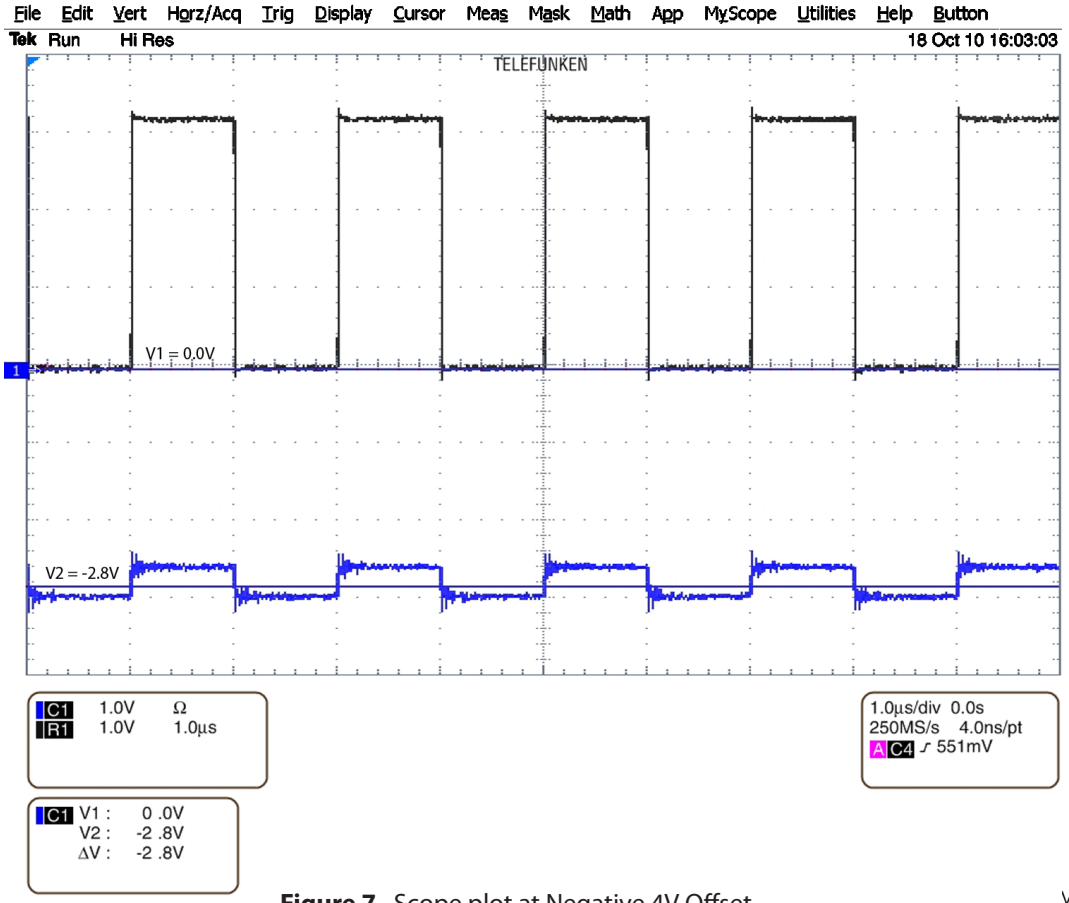


Figure 7. Scope plot at Negative 4V Offset

Figure 7 is a scope plot where GND1 is 4V less than GND2 The blue trace is V_A referenced to GND2 and the black trace is V_{output} referenced to GND2. As can been seen from the plot V_A reaches a minimum voltage of about -2.95V, well outside of the LVDS allowable voltage but, because of the wide common mode range capability of the TF90LVDS048 this is an appropriate input.

The V2 cursor is at -2.8V which is the V_{OS} of the TF90LVDS047 plus the -4.0V applied offset voltage(1.2 +(-4.0) = -2.8).

Figure 8 is a schematic of the voltage supplies that are connected to the TF90LVDS047_048EVK. Noted that since $V_{SUPPLY}2$ = -4.0V GND1 and GND2 may NOT be shorted together.

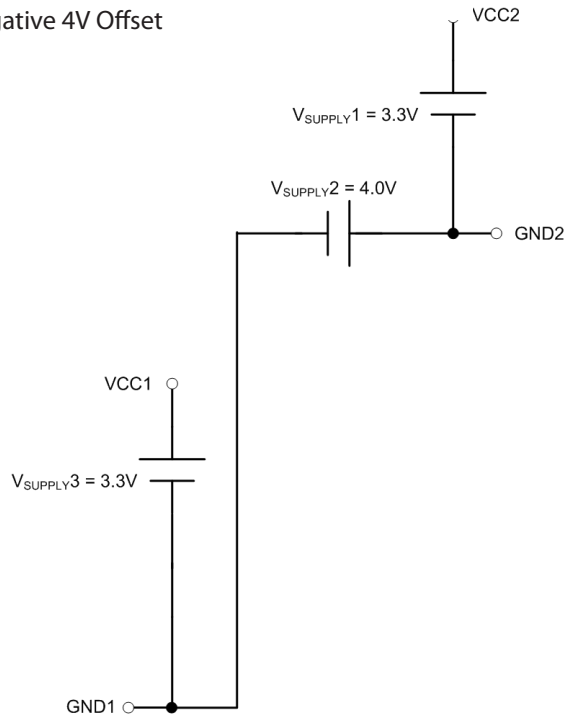


Figure 8. Negative 4V Offset applied to the Transmitter

Ground Loop

A ground loop is formed when two nets that are identified as grounds are at differing voltages and a conductor is placed between to two nets. As shown in Figure 6 and Figure 8 GND1 ≠ GND2 because of the offset voltage V2. Taking channel #4 of the TF90LVDS047_048EVK for example, it is routed to two 8-pin header where six of the eight pins of the header are connected to its local GND. If a ribbon cable was connected to the two 8-pin headers and GND1 ≠ GND2 current would flow from the GND with the highest potential to the GND with the lower potential through the ribbon cable and a ground loop will have been formed. If the power supplies are not current limited with current clamps or fuses and a ground loop is created there is a high probability that damage will occur.

Ground loops can be formed by other means as well. Figure 9 is an example of a ground loop being formed by earth grounds that are present in bench equipment. A data generator is connected to the input of the TF90LVDS047 and requires a return path or ground. The output of the TF90LVDS048 is connect to an oscilloscope and it requires a reference connection or ground. Both of these pieces of bench equipment connect these grounds to earth ground though their respective mains connection. If GND1 ≠ GND2 and these pieces of bench equipment are connected as shown a ground loop will be formed.

There are a number of options to eliminate these ground loops that are created by earth grounds in bench equipment. The data generator could be AC coupled to the input of the TF90LVDS047. This is accomplished by placing capacitors in series with the data generator and the TF90LVDS047. An isolation transformer could be used to connect the oscilloscope to an electrical outlet. This will allow the oscilloscope's ground to float and prevent a ground loop. (Note that the mains connection is not the only place where an earth ground might be present. It is also possible for communication cables such as GBIP to have ground connections through other pieces of bench equipment.) The method that was used for this document was a differential scope probe. Like other probes there are two connections at the input. Unlike standard scope probes there is not a low impedance ground connection but a high impedance negative connection. The information that is displayed on the scope is the difference between the positive input and the negative input of the differential scope probe. Therefore placing the negative input on GND2 and the positive input on the output of the TF90LVDS048 we are able to see the output relative to GND2 without causing a ground loop.

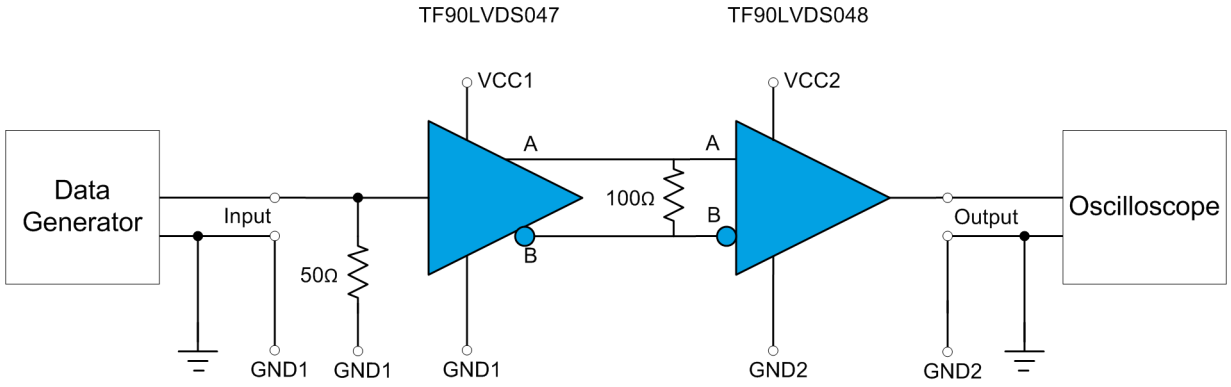
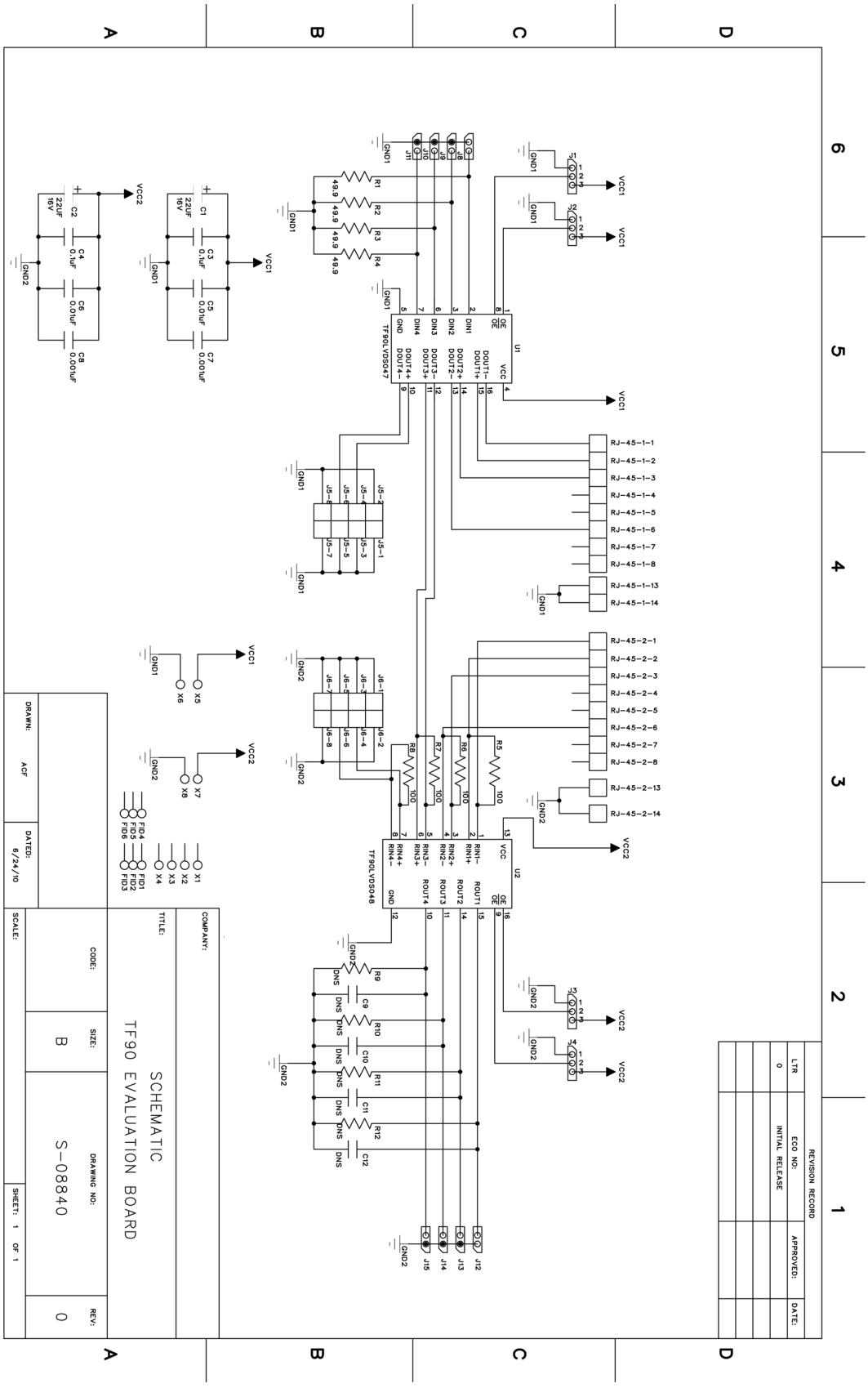


Figure 9. Ground loop formed by earth grounds

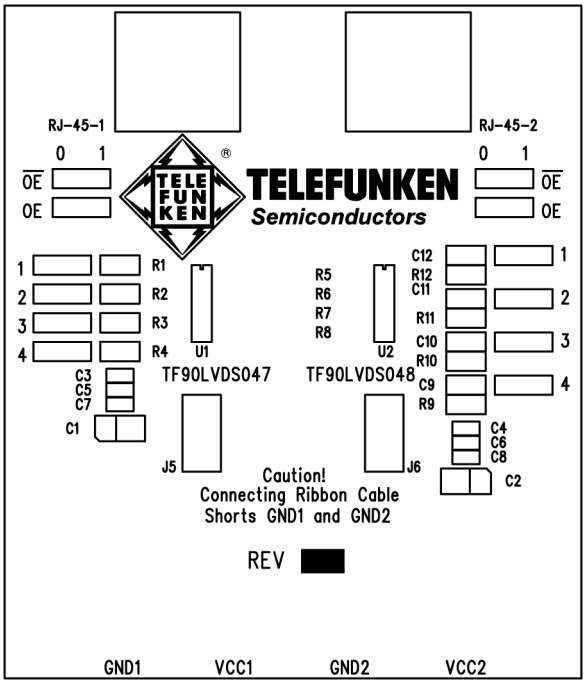
CAUTION!

All power supplies should be limited or fused at 100mA.
All power supplies must be capable of floating their negative outputs.

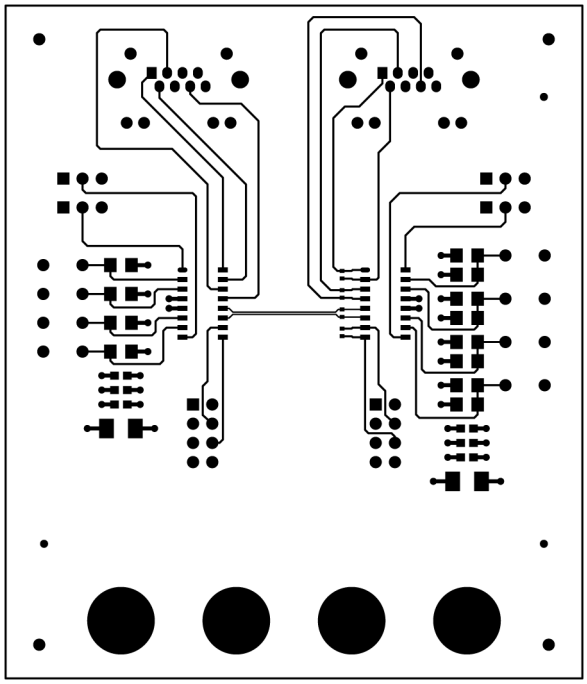
Schematic


TF90LVDS047
TF90LVDS048
RJ-45-1-1
RJ-45-1-2
RJ-45-1-3
RJ-45-1-4
RJ-45-1-5
RJ-45-1-6
RJ-45-1-7
RJ-45-1-8
RJ-45-1-13
RJ-45-1-14
RJ-45-2-1
RJ-45-2-2
RJ-45-2-3
RJ-45-2-4
RJ-45-2-5
RJ-45-2-6
RJ-45-2-7
RJ-45-2-8
RJ-45-2-13
RJ-45-2-14
TF90 EVALUATION BOARD
SCHEMATIC
S-08840
REVISION RECORD
INITIAL RELEASE

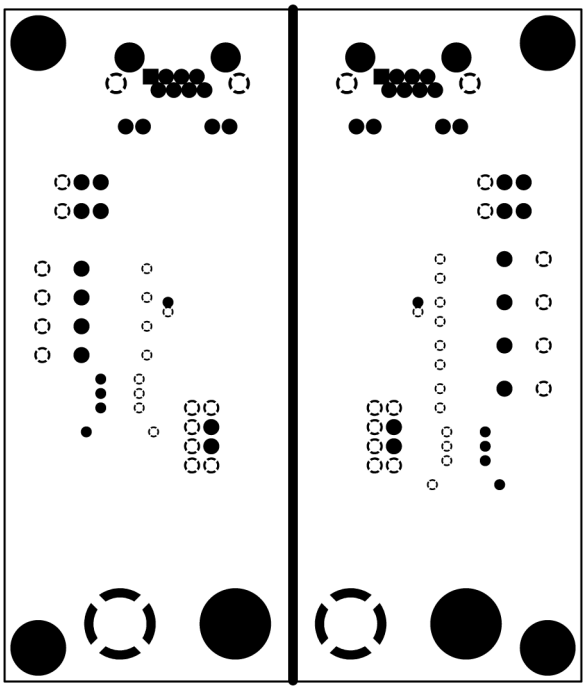
Layout



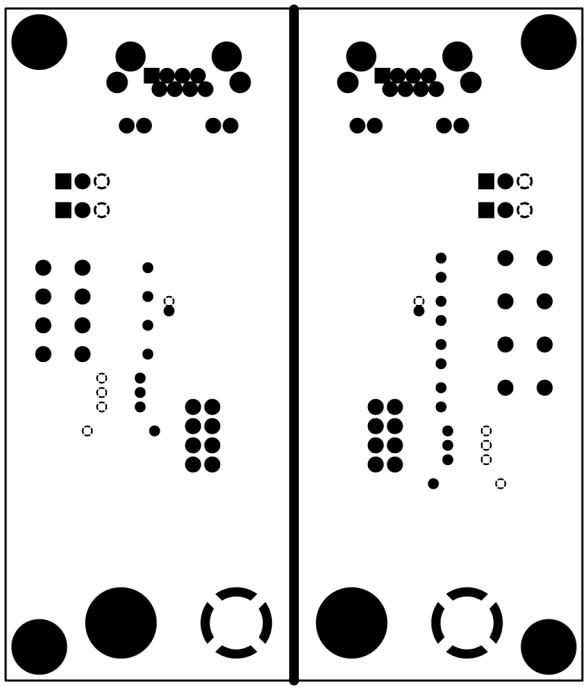
Silk Screen



Top Layer



GND1 and GND2 Layer



VCC1 and VCC2 Layer

Notes

Important Notice

For additional information please contact support@telefunkensemi.com or visit www.telefunkensemiconductors.com