TELEFUNKEN
Semiconductors

ADVANCE INFO

TFG1200

200V High-Side / Low-Side eGaN Gate Driver

Features

- Floating high-side driver in bootstrap operation to 200V
- 1.2A/5A peak source/sink current
- 0.4Ω/2Ω pull down/pull up impedance
- Internal bootstrap supply voltage clamped to 5.2V
- Independent high-side and low-side logic inputs
- Proprietary bootstrap capacitor auto-recharge technology
- Fast propagation delays (25ns typical)
- Separate source and sink outputs

Description

The TFG1200 is a high-side/low-side gate driver uniquely designed to drive enhancement mode Gallium Nitride (eGaN) FETs. The TFG1200 provides the special requirements of an eGaN FET driver: supply clamping, low pull-up and pull-down impedance, and high peak currents all within a single IC. A higher sink capability maintains the gate drive line at a low level during the fast dv/dt of the eGaN FET without unintended turn on of the FET. Fast propagation delays, fast rise times, and a proprietary bootstrap capacitor auto-recharge allow higher switching frequencies allowing smaller component footprints; and with the integrated bootstrap diode the required area compared to a discrete solution is greatly reduced.

Applications

- High Speed DC-DC Conversion
- Hard Switched and High Frequency Power Supplies
- Class D Audio

TDFN-10

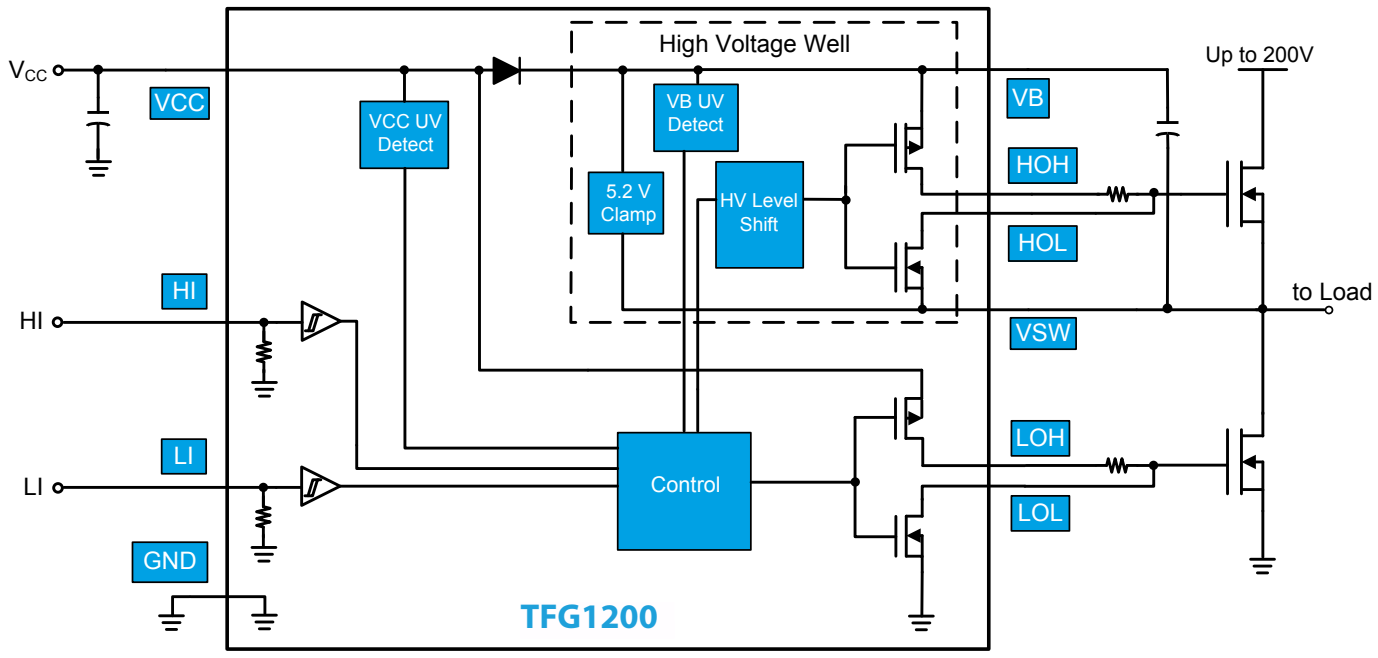
Ordering Information

Year Week Lot Lot

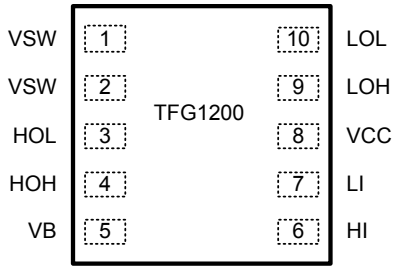
PART NUMBER (*NOTE1*)	PACKAGE	MARK	
		top	botm
TFG1200-NBX	TDFN-10	YWLL TBD	

NOTE1 *REPLACE* X *with* P *for 180 mm Tape & Reel Packing (Qty 3,000) or* Q *for 330 mm Tape & Reel Packing (Qty 10,000).*

Typical Application



Pin Diagrams



Top View: TDFN-10

(3x3mm, 10 pin, Pad Size: 1.8x2.5mm)

Pin Descriptions

PIN NAME	DFN PIN NUMBER	PIN DESCRIPTION
VSW	1	High-side bootstrap return
VSW	2	High-side bootstrap return
HOL	3	High-side gate driver sink output
HOH	4	High-side gate driver source output
VB	5	High-side bootstrap supply
HI	6	High-side gate driver control input
LI	7	Low-side gate driver control input
VCC	8	5V gate drive and control supply
LOH	9	Low-side gate driver source output
LOL	10	Low-side gate driver sink output
GND	PAD	Low-side and control ground

Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +207V
V_S - High side floating supply offset voltage.....V_B-7V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S/ dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Logic & low side fixed supply voltage.....-0.3V to +7V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V

V_{IN} - Logic input voltage (HI & LI).....-0.3V to +7V

P_D - Package power dissipation at $T_A \leq 25$ °C
TDFN-10.....TBD

TDFN-10 Thermal Resistance ***(NOTE2)***
θ_{JA}.....TBD °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

ESD Susceptibility
HBM ***(NOTE3)***.....2 kV
MM ***(NOTE4)***.....200 V
CDM ***(NOTE5)***.....1.5 kV

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE2 *Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.*
NOTE3 *Human Body Model, applicable standard JESD22-A114*
NOTE4 *Machine Model, applicable standard JESD22-A115*
NOTE5 *Field Induced Charge Device Model, applicable standard JESD22-C101*

Recommended Operating Conditions *(NOTE6)*

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 4$	$V_S + 5.5$	V
V_S	High side floating supply offset voltage	-5	200	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	4.5	5.5	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HI & LI)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE6 *Voltage amplitudes referenced to GND.*

DC Electrical Characteristics

All specifications at T_J = 25°C, V_{CC} = VB = 5V, VSW = GND = 0V, and no load on LOL, HOL, HOH, and HOL unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
I_{CCQ}	VCC quiescent current	LI=HI=0V		50		µA
I_{CCO}	VCC operating current	f=500kHz		0.5		mA
I_{VBQ}	VB quiescent current	LI=HI=0V		80		µA
I_{VBO}	VB operating current	f=500kHz		1.0		mA
T_J	Junction temperature		-40		200	°C
V_{IH}	Logic high input	Rising edge at LI and HI		3.8		V
V_{IL}	Logic low input	Falling edge at LI and HI		1.2		V
V_{IHYS}	Input hysteresis			2.5		V
V_{CCUV+}	VCC supply undervoltage positive going threshold			3.7		V
V_{CCUV-}	VCC supply undervoltage negative going threshold			3.5		V
V_{VBUV+}	VB supply undervoltage positive going threshold			3.7		V
V_{VBUV-}	VB supply undervoltage negative going threshold			3.5		V
$V_{BSClamp}$	VB – VSW clamp		4.7	5.2	5.5	V
V_{DL}	Bootstrap diode low-current forward voltage	I_{VCC-VB} = 100µA		0.6		V
V_{DH}	Bootstrap diode hi-current forward voltage	I_{VCC-VB} = 100µA		0.9		V
V_{DB}	Bootstrap diode breakdown voltage		200			V
R_{PU}	Gate driver pull up impedance	V_{SAT} = 100mV		1.7		Ω
R_{PD}	Gate driver pull down impedance	V_{SAT} = 100mV		0.4		Ω
I_{OH}	Peak source current	HOH=LOH=5V, C_L = 10nF		1.2		A
I_{OL}	Peak sink current	HOL=LOL=0V, C_L = 10nF		5		A
I_{OHLK}	High-level output leakage current	HOH=LOH=0V		1.5		µA
I_{OLLK}	Low-level output leakage current	HOL=LOL=5V		1.5		µA

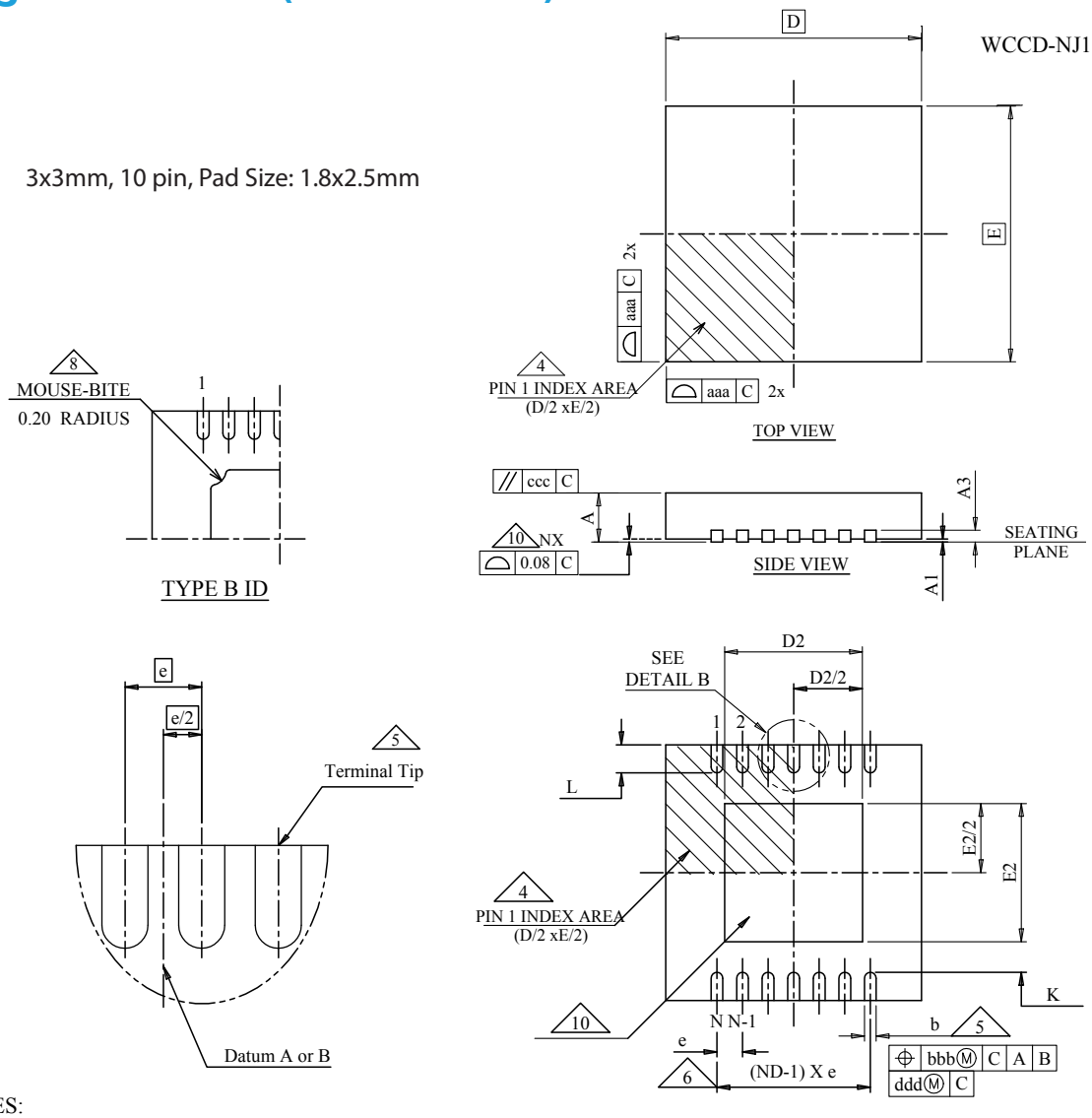
AC Electrical Characteristics

All specifications at $T_J = 25°C$, $V_{CC} = VB = 5V$, VSW = GND = 0V, and no load on LOL, HOL, HOH, and HOL unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{ONL}	LO turn-on propagation delay	LI rising to LOH rising		25		ns
t_{OFFL}	LO turn-off propagation delay	LI falling to LOL falling		25		ns
t_{ONH}	HO turn-on propagation delay	HI rising to HOH rising		25		ns
t_{OFFH}	HO turn-off propagation delay	HI falling to HOL falling		25		ns
$t_{DM\ ON}$	Delay matching: LO on & HO off			1.5		ns
$t_{DM\ OFF}$	Delay matching: LO off & HO on			1.5		ns
t_{HR}	HO rise time			7.0		ns
t_{LR}	LO rise time			7.0		ns
t_{HF}	HO fall time			1.5		ns
t_{LF}	LO fall time			1.5		ns
t_{PW}	Minimum input pulse width that changes the output			10		ns
t_{BS}	Bootstrap diode reverse recovery time	I_F = 100mA, I_R = 100mA		40		ns

Package Dimensions (TDFN-10 3x3)

3x3mm, 10 pin, Pad Size: 1.8x2.5mm



NOTES:

1. Dimensions in table are the TF4601, WCCD-NJ1 variation of the MLP Dual Family Package Outline.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. All dimensions are in millimeters, angle is in degrees (°).
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold, embeded metal or mark feature.
6. Dimension b applies to metallized terminal and is measured between 0.15MM and 0.30MM from terminal tip.
7. ND refers to the maximum number of terminals on D side.
8. For a complete set of dimensions for each variation, see the individual variation and the common dimensions and tolerances on page 4.
9. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
10. In the case of the rectangular package, the terminal side of the package is determined as followed:
    a) Type 1: The terminals are on the short side of the package.
    b) Type 2: The terminals are on the long side of the package.
11. Variation codes reference specific JEDEC MO-229 package variations. However, codes starting with NJR are not currently JEDEC registered and not defined in the 'Variation Designation' table. Variation with a star (*) symbol are also not JEDEC registered.
12. When more than one variation (option) exists for the same profile height, body size (DxE), and pitch then those variations will be denoted by an additional dash number (i.e. -1,-2, etc) designator to identify them. The new variations would be created from all or any of the following reasons : Terminal count, Terminal length and/or exposed pad sizes.
13. Variation with Exposed Tie Bars do not comply with JEDEC OUTLINE MO-229

Dimension		MIN	NOM	MAX
A	Height	0.70	0.75	0.80
D	Length		2.0	
E	Width		2.0	
A1		0.00	0.02	0.05
A3			0.20 Ref	
e	Pitch		0.50	
K			0.20	
b	Lead Width	0.18	0.25	0.30
D2	DAP Length	1.55	1.70	1.80
E2	DAP Height	0.75	0.90	1.00
L		0.20	0.30	0.40

Notes

Important Notice

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