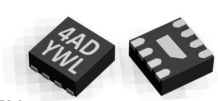
TELEFUNKEN Semiconductors

TF4602

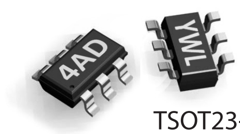
1.3 MHz Asynchronous Step-Up Regulator White LED Driver

Features

- **Drives white LED arrays, up to 13x3 in size, for display backlighting**
- **Wide input voltage range: 2.5V to 6V**
- **High efficiency enabled by an integrated 500 mΩ power MOSFET switch**
- **Low 104 mV internal reference voltage brings additional power savings**
- **Operates at fixed 1.3 MHz frequency for small filter size**
- **0.1 μA typical shut-down supply current**
- **Integrated soft-start function, 28V over-voltage protection, over-temperature protection and input under-voltage lockout**
- **Industrial temperature range: -40 °C to +85 °C**
- **Available in space saving DFN-8 and TSOT23-6 packages**



DFN-8

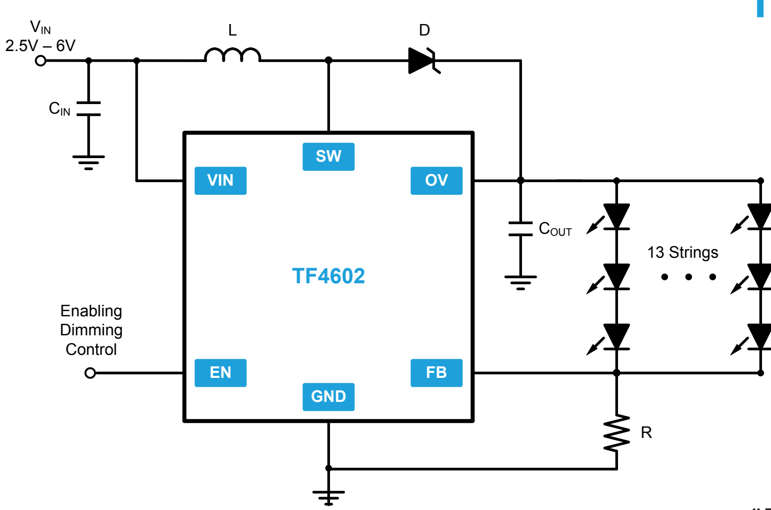


TSOT23-6

Applications

- White and Organic LED backlights
- Cellular Phones
- Digital Cameras
- PDAs, Smart Phones, MP3 Players
- Portable Instruments

Typical Application



Description

The TF4602 is a monolithic asynchronous boost regulator. An integrated 500 mΩ Power MOSFET drives up to 13 parallel strings of 3 WLEDs. It operates at fixed 1.3 MHz switching frequency, maximizing conversion efficiency, enabling smaller external components and reducing output ripple. Combined with a wide input voltage range of 2.5V to 6V the TF4602 is an ideal solution for portable electronic devices.

The TF4602 features an integrated soft-start function that minimizes inrush current during turn-on. Under-voltage lockout, over-voltage and over-temperature protection features are added for system robustness. It is available with an internal low voltage references of 104 mV for high efficiency. The current mode control loop is compensated internally minimizing the number of external components.

The TF4602 is offered in space saving 8-pin DFN and 6-pin TSOT23 packages. It operates over the industrial temperature range of -40 °C to +85 °C.

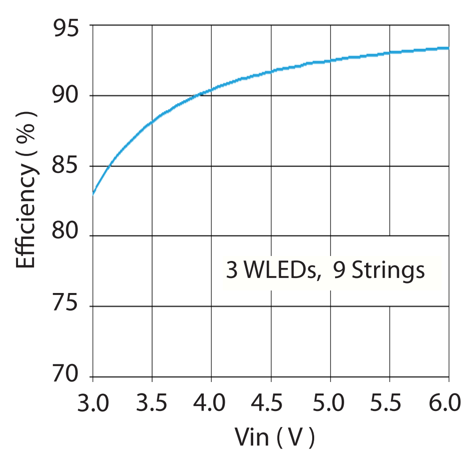
Ordering Information

Year Week Lot

PART NUMBER (*NOTE1*)	V_{FB}	V_{OV}	PACKAGE	MARK*	
				top	botm
TF4602-UTX	104mV	28V	TSOT23-6	4AD	YWL
TF4602-NBX	104mV	28V	DFN-8	4AD YWL	

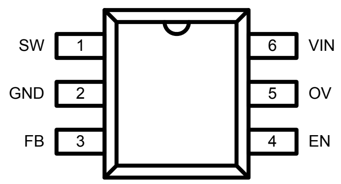
NOTE1 *REPLACE X with P for 180 mm Tape & Reel Packing (Qty 3,000) or Q for 330 mm Tape & Reel Packing (Qty 10,000).*

Typical Efficiency

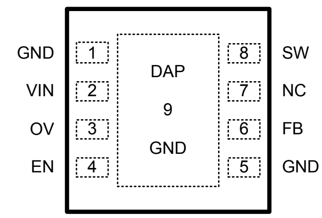


**For more information regarding Package Mark, please view package info at end of this document*

Pin Diagrams



Top View: TSOT23-6



Top View: DFN-8

Pin Descriptions

PIN NAME	SOT PIN NUMBER	DFN PIN NUMBER	PIN DESCRIPTION
SW	1	8	The drain of the internal power MOSFET switch. Connect the power inductor and output rectifier to this pin.
GND	2	1, 5, 9	Ground pin.
FB	3	6	Feedback input pin. The TF4602 regulates the voltage across the current sense resistor placed between the FB and GND pins. Connect the bottom of the LED string to the FB pin.
EN	4	4	Enable input pin. The EN pin is a digital input pin that enables or disables the regulator. When the EN is logic high, the regulator is turned ON. When the EN is logic low, the regulator is shut down. DO NOT leave the EN pin floating.
OV	5	3	Output over-voltage monitor pin. Connect the OV pin to the output at the top of the LED string.
VIN	6	2	Power input pin. The IN pin supplies the power to the IC and the step-up converter switch.
NC	-	7	"No Connect" pin.

Absolute Maximum Ratings *(NOTE2)*

V_{IN} - Supply input pin voltage ....-0.3V to +6.5V
V_{SW} - Switching pin voltage ....-0.5V to +28.5V
V_{OV} - Over-voltage monitor pin voltage ....-0.5V to +28.5V
All other pins ....-0.3V to +6.5V

DFN-8 Thermal Resistance ***(NOTE3)***

θ_{JC}...16 °C/W
θ_{JA}...80 °C/W

SOT-23-6 Thermal Resistance ***(NOTE3)***

θ_{JC}...110 °C/W
θ_{JA}...220 °C/W

T_J - Junction operating temperature ....+150 °C
T_L - Lead temperature (soldering, 10s) .... +260 °C
T_{stg} - Storage temperature range ....-65 °C to +150 °C

Recommended Operating Conditions

V_{IN} - Input voltage ....2.5V to 6V
T_A - Operating ambient temperature range..........-40 °C to +85 °C
T_J - Junction temperature range.............................-40 °C to +125 °C

NOTE2 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
NOTE3 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Electrical Characteristics

T_A = 25 °C, V_{IN} = 5V, unless otherwise specified.

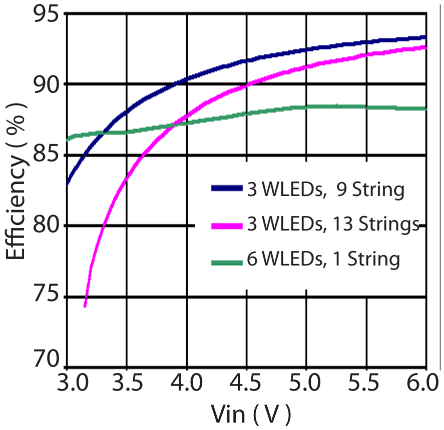
Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input voltage		2.5		6.0	V
V_{UVLO}	Under-voltage lockout	V_{IN} rising		2.25	2.45	V
$V_{UVLOhyst}$	UVLO hysteresis			0.1		V
I_Q	Quiescent current	V_{FB} = 0.15V, Not Switching		690	750	µA
I_{IN}	Supply current	V_{FB} = 0V, Switching		1	2	mA
I_{SHDN}	Shut-down current	V_{EN} = 0V		0.1	1	µA
$R_{DS(ON)}$	Switch ON resistance			0.5	1.0	Ω
V_{FB}	Feedback voltage		94	104	114	mV
I_{FB}	Feedback input bias current	V_{FB} = 0.1V	-600	-300		nA
	Line regulation	V_{IN} = 3V to 4.3V ***(NOTE4)***		1		%
	Load regulation	I_{OUT} = 1 mA to 180 mA ***(NOTE5)***		1		%
f_{osc}	Oscillator frequency		1.0	1.3	1.5	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0V	85	92		%
V_{IH}	Enable input logic high voltage	V_{EN} Rising, V_{IN} = 5V	1.6			V
V_{IL}	Enable input logic low voltage	V_{EN} Rising, V_{IN} = 5V			1.0	V
		V_{EN} Rising, V_{IN} = 2.5V			0.8	
I_{IN}	Enable input current	V_{EN} = 0V, 5V			1	µA
V_{ENhyst}	Enable input threshold voltage hysteresis			90		mV
V_{OVP}	Output over-voltage threshold	V_{OVP} rising	26	28	30	V
I_{OCP}	Over-current threshold	60% duty cycle	1	1.33		A
T_{OTP}	Over-temperature threshold			160		°C
$T_{OTPhyst}$	Over-temperature threshold hysteresis			30		°C

NOTE4 *Line regulation is measured on the system illustrated in Figure 1 with the following component values and loading:* C_{IN} = 2.2 µF, C_{OUT} = 1 µF, I_{OUT} = 180 mA, L = 10 µH.

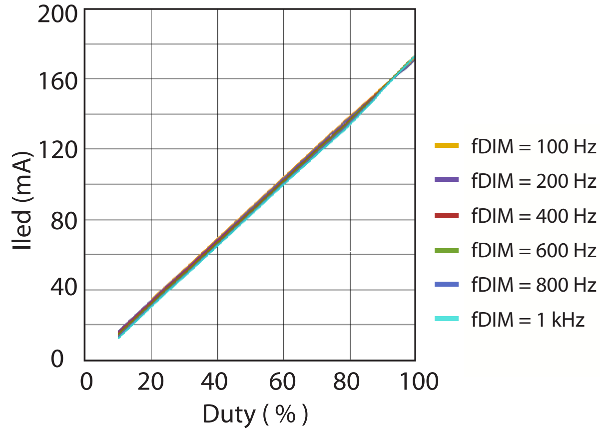
NOTE5 *Load regulation is measured on the system illustrated in Figure 1 with the following component values:* C_{IN} = 2.2 µF, C_{OUT} = 1 µF, L = 10 µH.

Typical Performance Characteristics

Efficiency vs Input Voltage
TF4602

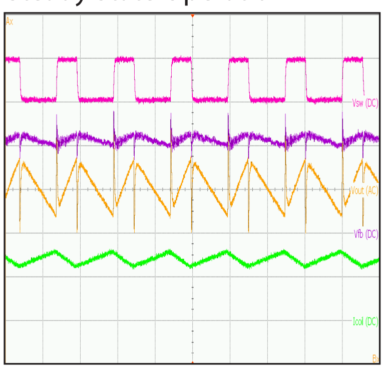


Output Current vs
PWM Dimming Duty
VIN = 5V, 3WLEDs, 180mA



Vin = 3.7V, 3 WLEDs 13 String

Steady State Operation



500 ns/Div

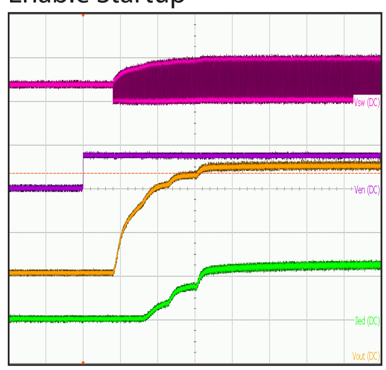
Vsw = 10V/div

Vfb = 50mV/div

Vout = 100mV/div
(AC coupled)

Icoil = 500mA/div

Enable Startup



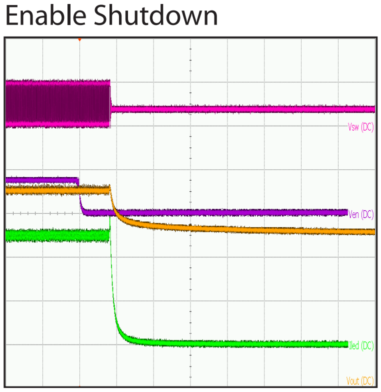
50 µs/Div

Vsw = 10V/div

Ven = 5V/div
Vout = 2V/div

Iled = 200mA/div

Enable Shutdown



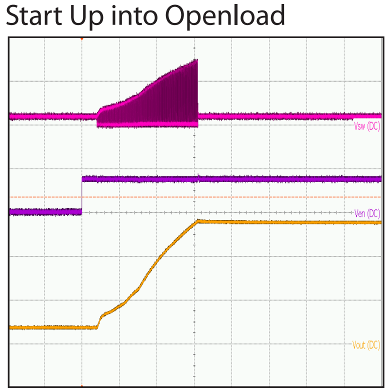
50 µs/Div

Vsw = 10V/div

Ven = 5V/div
Vout = 2V/div

Iled = 100mA/div

Start Up into Openload



1 ms/Div

Vsw = 20V/div

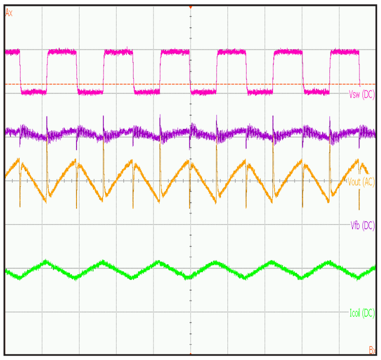
Ven = 5V/div

Vout = 10V/div

Typical Performance Characteristics

Vin = 5V, 3 WLEDs 13 String

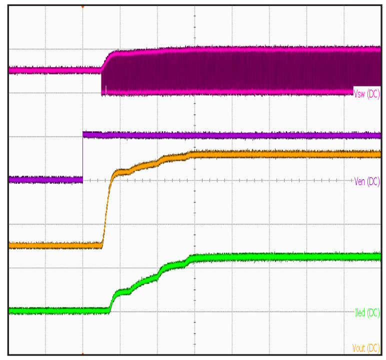
Steady State Operation



Vsw = 10V/div
Vfb = 50mV/div
Vout = 100mV/div (AC coupled)
Icoil = 500mA/div

500ns/Div

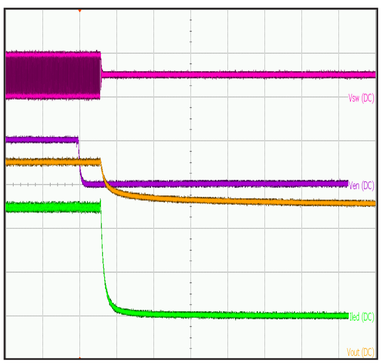
Enable Startup



Vsw = 10V/div
Ven = 5V/div
Vout = 2V/div
Iled = 200mA/div

50 µs/Div

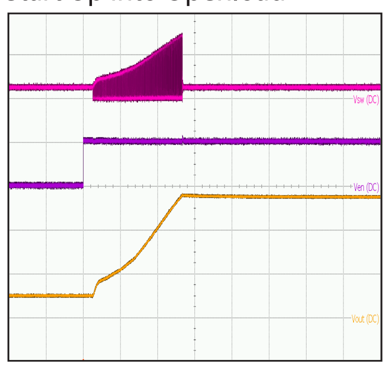
Enable Shutdown



Vsw = 10V/div
Ven = 5V/div
Vout = 2V/div
Iled = 100mA/div

50µs/Div

Start Up into Openload



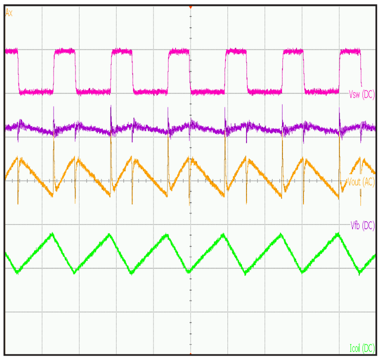
Vsw = 20V/div
Ven = 5V/div
Vout = 10V/div

100 µs/Div

Typical Performance Characteristics

Vin = 3.7V, 3 WLEDs 9 String

Steady State Operation



Vsw = 10V/div

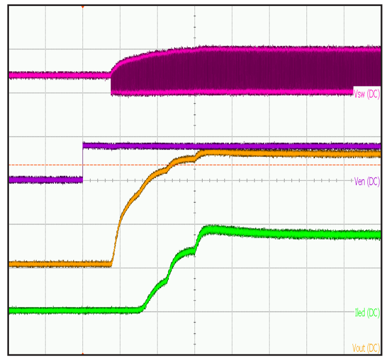
Vfb = 50mV/div

Vout = 100mV/div (AC coupled)

Icoil = 200mA/div

500ns/Div

Enable Startup



Vsw = 10V/div

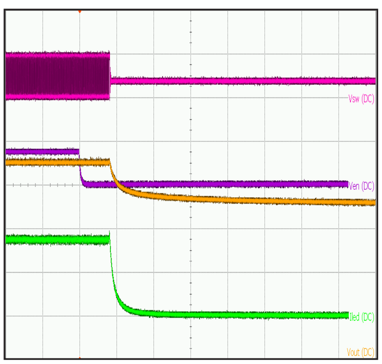
Ven = 5V/div

Vout = 2V/div

Iled = 100mA/div

50 µs/Div

Enable Shutdown



Vsw = 10V/div

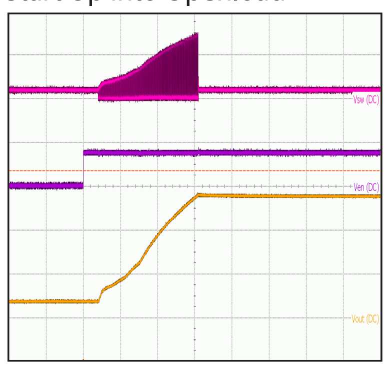
Ven = 5V/div

Vout = 2V/div

Iled = 100mA/div

50µs/Div

Start Up into Openload



Vsw = 20V/div

Ven = 5V/div

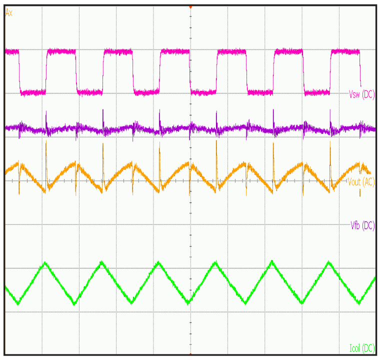
Vout = 10V/div

100 µs/Div

Typical Performance Characteristics

Vin = 5V, 3 WLEDs 9 String

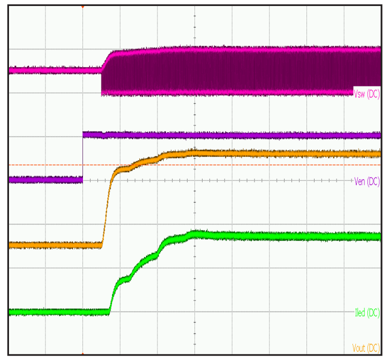
Steady State Operation



Vsw = 10V/div
Vfb = 50mV/div
Vout = 100mV/div (AC coupled)
Icoil = 200mA/div

500ns/Div

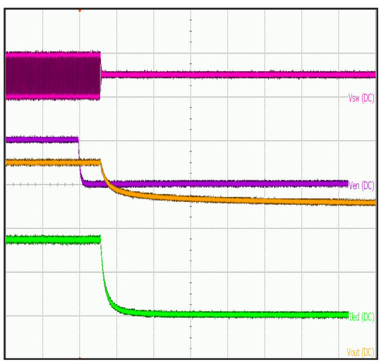
Enable Startup



Vsw = 10V/div
Ven = 5V/div
Vout = 2V/div
Iled = 100mA/div

50 µs/Div

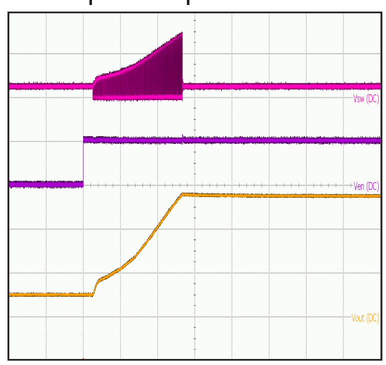
Enable Shutdown



Vsw = 10V/div
Ven = 5V/div
Vout = 2V/div
Iled = 100mA/div

50µs/Div

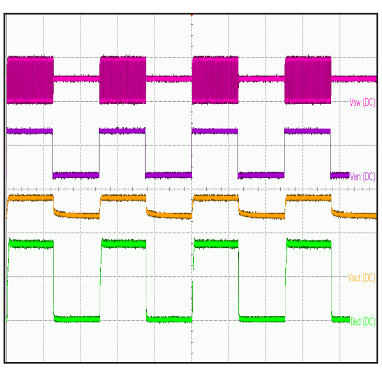
Start Up into Openload



Vsw = 20V/div
Ven = 5V/div
Vout = 10V/div

100 µs/Div

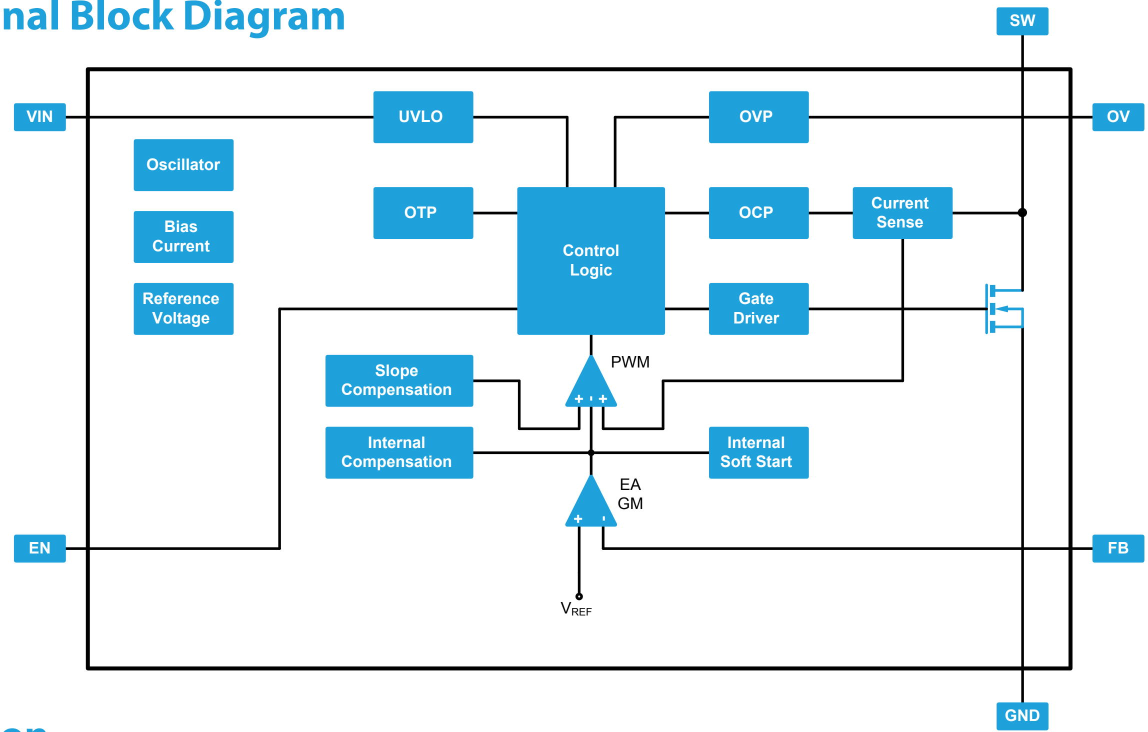
PWM Dimming
f=200Hz, DC = 50%



Vsw = 10V/div
Ven = 5V/div
Vout = 5V/div
Iled = 100mA/div

2 ms/Div

Functional Block Diagram



Operation

The TF4602 is an integrated current mode step-up regulator switching at a fixed frequency of 1.3MHz. To get an overview of the operation refer to the functional block diagram.

At the beginning of every cycle, the Power MOSFET is turned on which leads to an increasing current through the external inductor and likewise through the MOSFET. This current flow is sensed and the sense signal is delivered to the PWM comparator, to which a stabilizing ramp ("Slope Compensation") is added to prevent sub-harmonic oscillation. These two signals are compared to the output voltage of the error amplifier: When the sum of slope compensation and current sense signal crosses the error amplifier output voltage, the control logic will make the Power MOSFET turn off for the rest of the cycle.

The error amplifier compares the internal reference voltage (104mV) with the voltage at the feedback pin. If the feedback voltage is lower than the reference voltage, the circuit will increase the duty cycle of the Power MOSFET until the feedback voltage reaches the reference voltage. Inversely if the feedback voltage is too high, the circuit will reduce it's duty cycle until the correct feedback voltage is reached again.

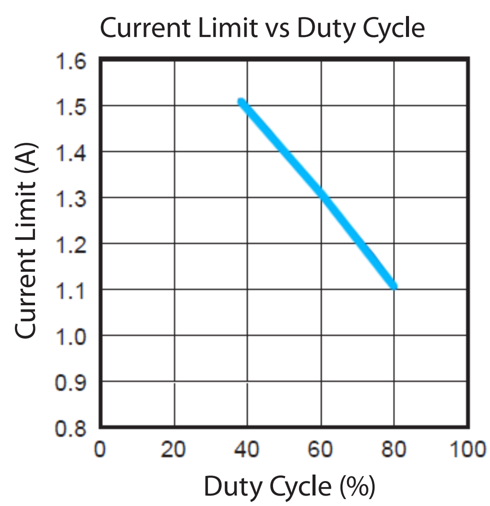
The stabilizing ramp added to the current sense signal reduces the current output as the duty cycle increases: As more LEDs are added to the string, the output voltage rises. Therefore the duty cycle has to be increased and the maximum current that can be delivered to the load is reduced as well (see graph on right side).

The TF4602 has internal soft-start to limit the amount of current through the IN pin at startup and to also limit the amount of overshoot on the output. The current limit is increased by a fourth every 40 µs giving a total soft-start time of 120 µs.

The enable pin can also be used for dimming. The device will turn on and off with the enable signal frequency and duty cycle. Due to the 120µs soft start period, a dimming frequency of 1kHz or lower is recommended to get a good dimming accuracy.

Dimming frequencies below 80Hz should be also avoided to prevent visible flickering.

Open Load protection will shut off the TF4602 if the output voltage rises to high when the OV pin is tied to the output. In some cases an LED may fail, which will result in a short or an open. In case of an open, the feedback voltage will always remain at zero. The part will run at maximum duty cycle boosting the output voltage higher and higher. By tying the OV pin to the top of the LED string, the TF4602 can check for this condition. If the output exceeds 28V, the TF4602 will shut down. The part will not start switching again until the power is recycled.



Application Information

This section of the data sheet describes typical application circuits and provides recommendations on dimming control and component selection.

TYPICAL APPLICATIONS

The TF4602 uses a fixed frequency, current-mode step-up regulator architecture to drive arrays of white LEDs. Figure 1 shows a typical application circuit.

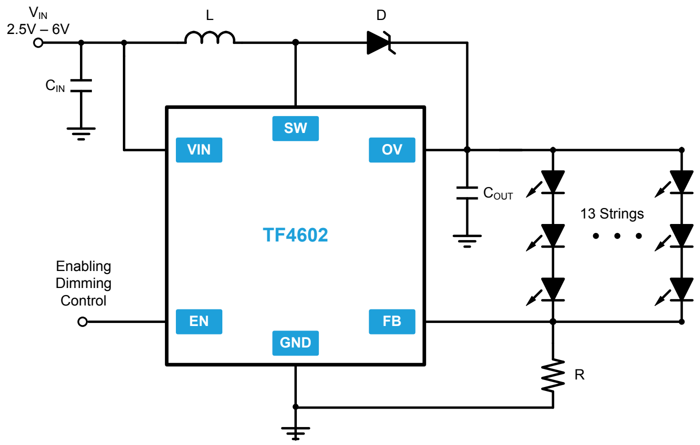


Figure 1. Typical Application Circuit

The circuit of Figure 1 can drive various topologies of white LEDs ranging from 3x1 arrays to 3x13 arrays. The component selection may vary for each topology depending on the V_{OUT} / V_{IN} ratio and the LED current requirements. This is discussed in the later subsections of the Application Information.

SETTING THE LED CURRENT

Based on the circuit of Figure 1, the LED current depends on the reference voltage, V_{REF}, and the resistor, R_{SET}, as expressed with the following equation:

$$I_{LED} = \frac{V_{REF}}{R_{SET}}$$

Table 1 exemplifies several standard resistor values needed for a given LED current. If standard resistor values are not available a parallel combination of two standard resistors may also be used to get the desired LED current.

V_{REF} [mV]	I_{LED} [mA]	R_{SET} [Ω]
104	10	10.5
	20	5.23
	100	1.05
	180	1.2 || 1.1
	260	0.4

Table 1. Examples of Standard Value Resistors for a Given LED Current

Component Selection

Inductor: High frequency operation of the TF4602 allows the use of small surface mount inductors. The minimum inductance value is inversely proportional to the operating frequency and is bounded by the following limits:

$$L > \frac{3}{f}[\mu H] \wedge L > \frac{V_{IN(MIN)} \bullet (V_{OUT(MAX)} - V_{IN(MIN)})}{f \bullet I_{L(MAX)ripple} \bullet V_{OUT(MAX)}}[H]$$

where

- f = Operating frequency [Hz]
- $I_{L(MAX)ripple}$ = Allowable maximum inductor current ripple [A]
- $V_{IN(MIN)}$ = Minimum input voltage [V]
- $V_{OUT(MAX)}$ = Maximum output voltage [V]

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current. Given this, the operating frequency and the input and output voltage ranges for the TF4602 regulator circuits, it is easy to calculate the optimal inductor value which typically ranges between 10 and 47 µH.

For high efficiency, it is recommended to select an inductor with a high frequency core material (e.g. ferrite) to minimize core losses. Low ESR (equivalent series resistance) is another preferred inductor characteristic when designing for low losses. The inductor must handle the peak inductor current at full load without saturating. Chip inductors typically do not have enough core to support the peak inductor currents above 1A and are not suitable for the TF4602 applications. Lastly, select a toroid, pot core or shielded bobbin inductor for low radiated noise. Table 2 provides a list of recommended inductor series.

Inductor Series	Supplier	Website
SRU8043	Bourns Inc.	www.bourns.com
MSS7341	Coilcraft	www.coilcraft.com
LQH88P	Murata	www.murata.com
DR1040	Coiltronics	www.coiltronics.com
CDRH8D43	Sumida	www.sumida.com

Table 2. List of Recommended Inductor Series

Input Capacitor: The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. The input capacitor values in the range between 2.2 and 4.7 µF are sufficient in most cases. Ceramic, low ESR capacitors are recommended for a low loss operation.

Output Capacitor: The value of the output capacitor has an effect on the output voltage ripple as expressed in the following equation:

$$V_{ripple(BULK)} = \frac{I_{L(peak)} \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f}[V]$$

where

- f = Operating frequency [Hz]
- $I_{L(peak)}$ = Peak inductor current [A]
- $V_{IN(MIN)}$ = Input voltage [V]
- $V_{OUT(MAX)}$ = Output voltage [V]

Another significant component of the output voltage ripple is the ripple due to the capacitor ESR. This components is simply expressed in the following equation:

$$V_{ripple(ESR)} = I_{L(peak)} \bullet ESR_{COUT}[V]$$

The output capacitor values in the range between 1.0 and 2.2 µF provide low output voltage ripple in most cases. Table 3 provides a list of recommended capacitor series.

Capacitor Series	Supplier	Website
0201-2225 Ceramic TPS, TPM Tantalum	AVX	www.avx.com
MK107, MK212, MK316 Ceramic	Taiyo Yuden	www.t-yuden.com
POSCAP Electrolytic	Sanyo	edc.sanyo.com

Table 3. List of Recommended Capacitor Series

Output Diode: The primary function of the output diode is to protect the TF4602 V_{IN} pin when the output voltage is above the absolute maximum voltage rating of the pin (6.5V). Schottky diodes feature low forward voltage and fast recovery times that result in improved peak efficiency of the boost regulator circuits. Table 4 provides a list of recommended diode series.

Diode Series	Supplier	Website
MBR0520-80	MCC	www.mccsemi.com
SBR	Diodes Inc.	www.diodes.com
SS1P3	Vishay	www.vishay.com

Table 4. List of Recommended Schottky Diode Series

Dimming Control

There are three popular methods to control dimming for the TF4602 white LED driver circuits. The details of each method follow.

Using a PWM Logic Signal: Dimming control using a PWM logic signal is shown in Figure 2.

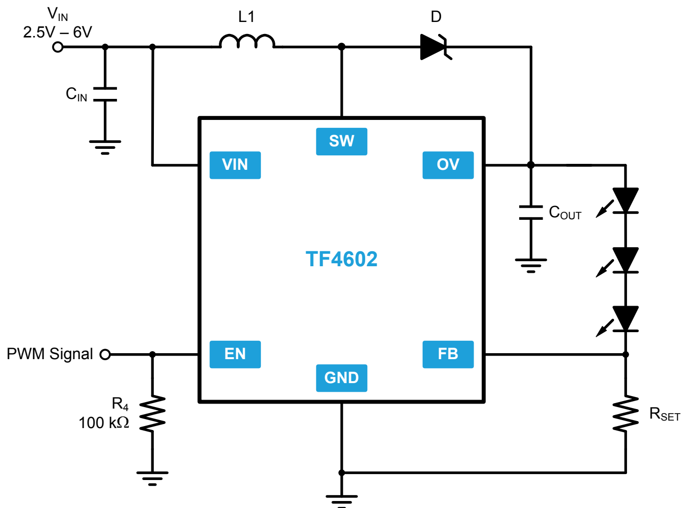


Figure 2. Dimming Control Using a PWM Logic Signal

The PWM logic signal is applied to the EN pin of the TF4602. The average I_{LED} is directly proportional to the DCD of the PWM logic signal. The frequency of the signal should be 1 kHz or lower due to the soft-start function.

Using a DC Voltage: Dimming control using a variable DC voltage is shown in Figure 3.

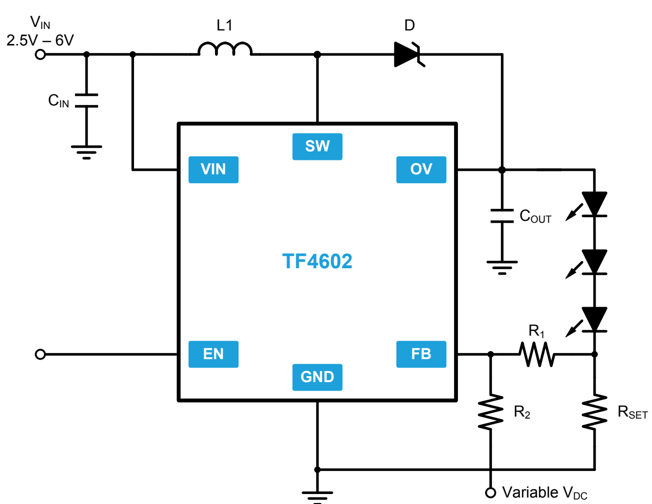


Figure 3. Dimming Control Using a Variable DC Voltage

As the DC voltage increases, the current through the R_1 increases. The higher the I_{R1}, the lower the I_{LED} as the control loop is now regulating the sum of the I_{R1} and I_{LED}. The I_{LED} can be calculated using the following equation:

$$I_{LED} = \frac{V_{REF} - \frac{R_1 \bullet (V_{DC} - V_{REF})}{R_2}}{R_{SET}} [A]$$

As an example, if the V_{DC} is varied between 0V and 2.0V, the selection of R_1 =5 kΩ, R_2 = 90 kΩ and R_{SET} = 5.23Ω sets the I_{LED} between approximately 21 mA and 0 mA for the TF4602 (V_{REF} = 104 mV).

Using a Filtered PWM Signal: Dimming control using a filtered PWM signal is another popular method for LED dimming control and is show in Figure 4. In this method, a filtered PWM signal acts as the DC voltage to regulate the output current. The I_{LED} can be calculated using the following equation:

$$I_{LED} = \frac{V_{REF} - \frac{R_1 \bullet (V_{PWM} \bullet DCD - V_{REF})}{R_2 + R_3}}{R_{SET}} [A]$$

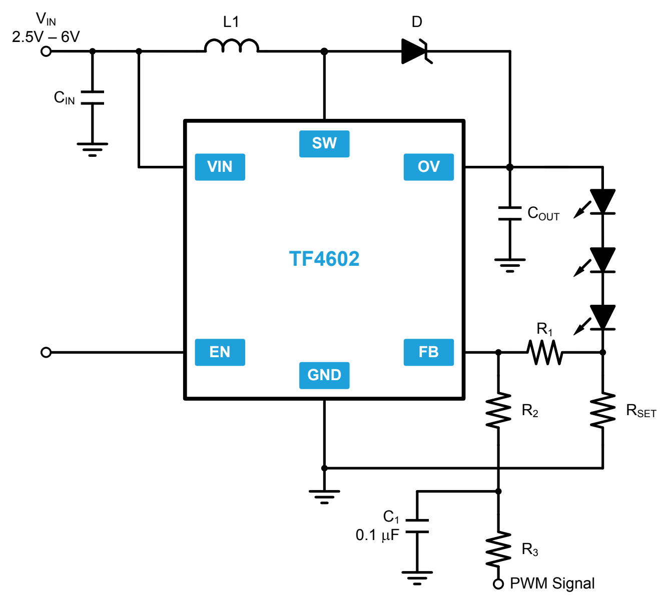


Figure 4. Dimming Control Using a Filtered PWM Signal

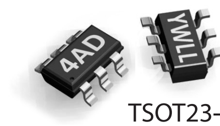
The PWM signal in the circuit of Figure 4 affects the output voltage ripple. To minimize this effect, recommended frequency of the signal is 1 kHz or greater.

PCB Layout Considerations

When using DC-DC switching power converters, a carefully designed PCB layout is mandatory.

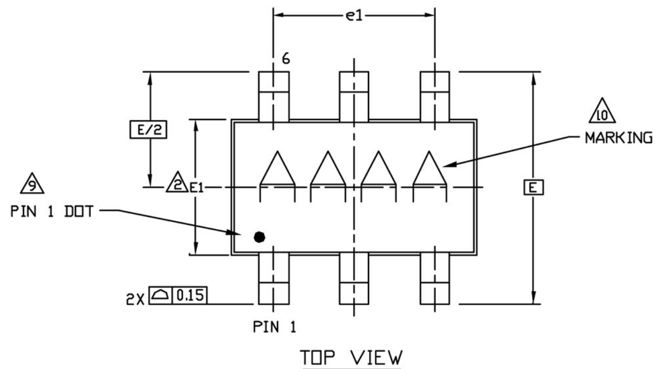
1. Because of the fast switching slopes, the wire areas and lengths between switching pins and connected components have to be small, to keep noise and electromagnetic interference as low as possible. Therefore place the inductor and rectifying diode preferably close to the switch pin.
2. Sensitive high ohmic nodes may not be placed close to high current and/or switching paths. For example keep the feedback net away from the switching node. Also keep it short and as close to the chip as possible. If it's feasible, use ground paths to shield these sensitive lines.
3. Place the input capacitor as close to the chip as possible. The output capacitor should be placed as close to the cathode of the rectifying diode as possible. Make sure that input and output capacitor are well connected at the ground side.
4. To keep the switching ripple on the input and output voltage low, use low ESR ceramic bypass capacitors.
5. Keep in mind the voltage- and temperature dependency of capacitor types. Therefore X5R and X7R capacitors are highly recommended as input and output capacitors.
6. Take care of possible ground shift! To avoid unwanted ground shift that may have disturbing effects on the regulation loop, a big ground plane is recommended. For optimal performance, use a PCB board with at least two metal layers, so that one of the layers can be used as a ground plane.
7. Consider high current paths. The connection between input board connector, input cap and inductor as well as the connection between output board connector, output cap and rectifying diode and the connection between inductor, rectifying diode and switch pin have to be wide enough to avoid unwanted voltage drop caused by parasitic resistance.

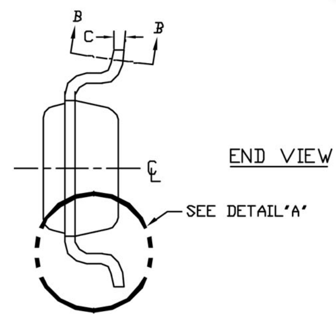
Package Dimensions (TSOT23-6) and Package Mark

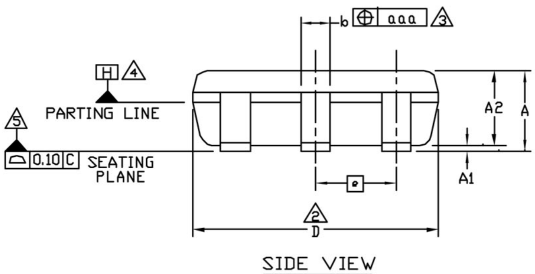


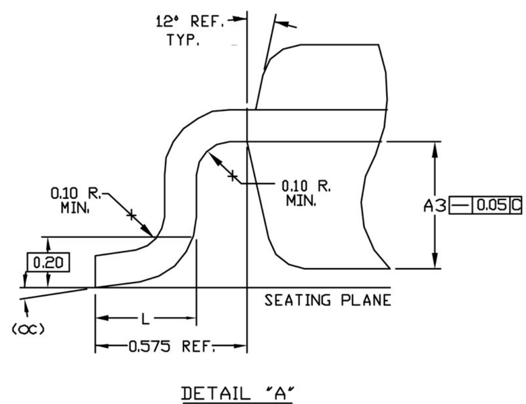
TSOT23-6

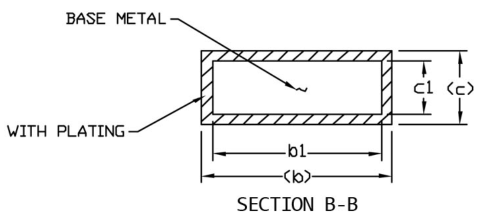
Package Mark after Dec 1st, 2011









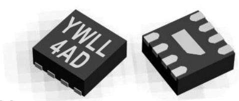


NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. (2) "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. (3) THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. (4) DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. (5) THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. (9) THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. (10) MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

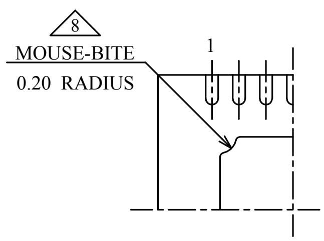
SYMBOLS	MIN	NOM	MAX
A	–	–	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
b	0.30	–	0.45
b1	0.25	0.35	0.40
c	0.15	–	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
α	0°	4°	8°
aaa		0.20	

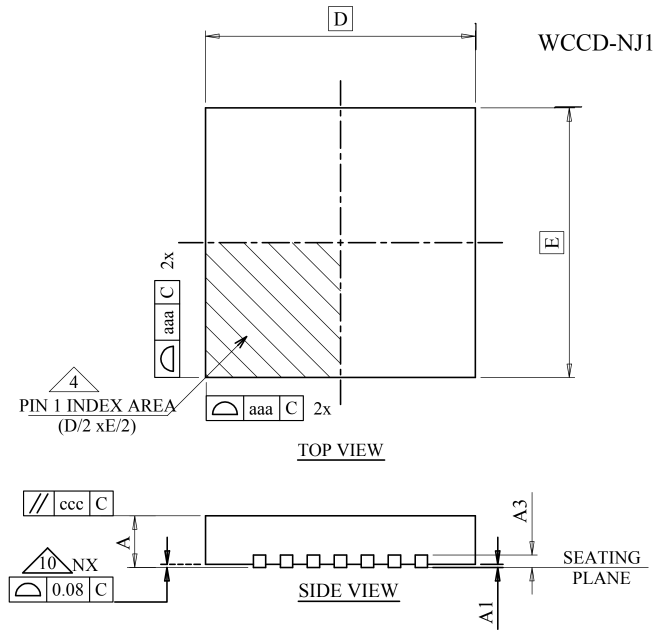
Package Dimensions (DFN-8 2x2) and Package Mark

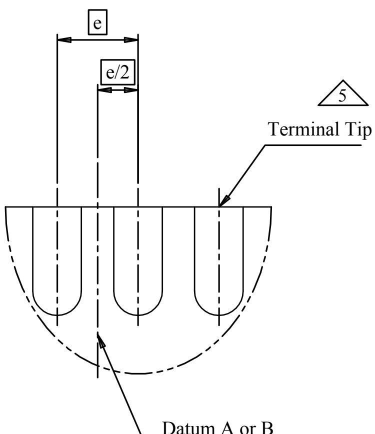


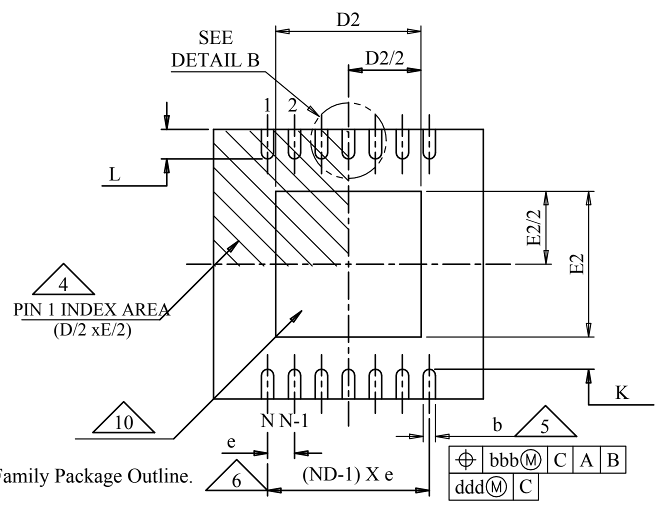
DFN-8

Package Mark after
Dec 1st, 2011









NOTES:

1. Dimensions in table are the TF4601, WCCD-NJ1 variation of the MLP Dual Family Package Outline.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. All dimensions are in millimeters, angle is in degrees (°).
4. N is the total number of terminals.
5. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The terminal #1 identifier may be either a mold, embeded metal or mark feature.
6. Dimension b applies to metallized terminal and is measured between 0.15MM and 0.30MM from terminal tip.
7. ND refers to the maximum number of terminals on D side.
8. For a complete set of dimensions for each variation, see the individual variation and the common dimensions and tolerances on page 4.
9. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
10. In the case of the rectangular package, the terminal side of the package is determined as followed:
    a) Type 1: The terminals are on the short side of the package.
    b) Type 2: The terminals are on the long side of the package.
11. Variation codes reference specific JEDEC MO-229 package variations. However, codes starting with NJR are not currently JEDEC registered and not defined in the 'Variation Designation' table. Variation with a star (*) symbol are also not JEDEC registered.
12. When more than one variation (option) exists for the same profile height, body size (DxE), and pitch then those variations will be denoted by an additional dash number (i.e. -1,-2, etc) designator to identify them. The new variations would be created from all or any of the following reasons : Terminal count, Terminal length and/or exposed pad sizes.
13. Variation with Exposed Tie Bars do not comply with JEDEC OUTLINE MO-229

Dimension		MIN	NOM	MAX
A	Height	0.70	0.75	0.80
D	Length		2.0	
E	Width		2.0	
A1		0.00	0.02	0.05
A3			0.20 Ref	
e	Pitch		0.50	
K			0.20	
b	Lead Width	0.18	0.25	0.30
D2	DAP Length	1.55	1.70	1.80
E2	DAP Height	0.75	0.90	1.00
L		0.20	0.30	0.40

Notes

Important Notice

Telefunken Semiconductors PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC Telefunken Semiconductors PRODUCTS ARE SPECIFICALLY DESIGNATED BY Telefunken Semiconductors FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF Telefunken Semiconductors PRODUCTS WHICH Telefunken Semiconductors HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER'S RISK.

Telefunken Semiconductors assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using Telefunken Semiconductors products.

Resale of Telefunken Semiconductors products or services with statements different from or beyond the parameters stated by Telefunken Semiconductors for that product or service voids all express and any implied warranties for the associated Telefunken Semiconductors product or service. Telefunken Semiconductors is not responsible or liable for any such statements.

For additional information please contact support@telefunkensemi.com or visit www.telefunkensemiconductors.com