



TF2110 / TF2113

High-Side and Low-Side Gate Drivers

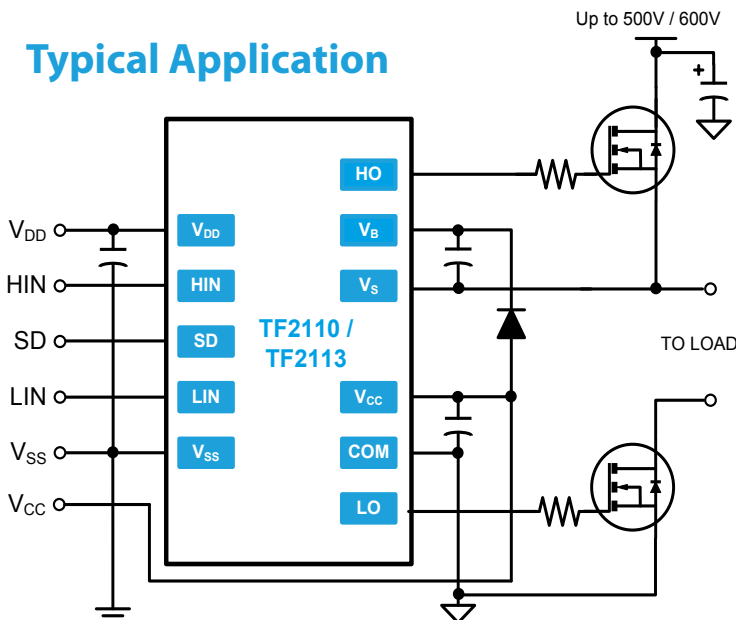
Features

- Drive two N-channel MOSFETs or IGBTs in high-side / low side configuration
- The floating high-side, drivers drive gates operating at up to 500V / 600V
- 2.5A sink / 2.5A source typical output currents
- Outputs tolerant to negative transients
- Wide gate driver supply voltage range: 10V to 20V
- Wide logic input supply voltage range: 3.3V to 20V
- Wide logic supply offset voltage range: -5V to 5V
- 10 ns (TF2110) / 20 ns (TF2113) maximum delay matching
- 27 ns (typ) rise / 17 ns (typ) fall times with 1000 pF load
- 120 ns (typ) turn-on / 94 ns (typ) turn-off delay times
- Under-voltage lockout for high- and low-side drivers
- Cycle-by-cycle edge-triggered shutdown circuitry
- Extended temperature range: -40 °C to +125 °C
- Drop-in replacements for IR2110 / IR2113

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Typical Application



Description

The TF2110 and TF2113 are high voltage, high-speed MOSFET and IGBT drivers with independent high-side and low-side outputs. The high-side driver features floating supply for operation at up to 500V / 600V. The 10 ns (max) / 20 ns (max) propagation delay matching between the high and the low side drivers allows high frequency operation.

The TF2110 and TF2113 logic inputs are compatible with standard CMOS levels (as low as 3.3V) while driver outputs feature high pulse current buffers designed for minimum driver cross-conduction.

The TF2110 and TF2113 are offered in 16-pin SOIC wide and 14-pin PDIP packages. They operate over an extended -40 °C to +125 °C temperature range.



PDIP-14



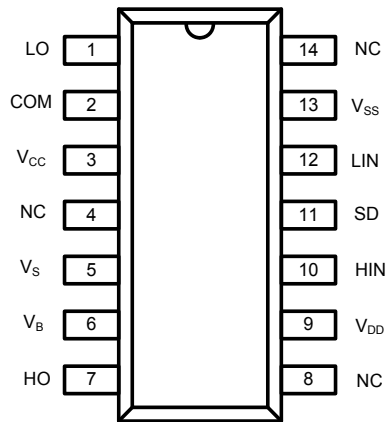
SOIC-16W

Year Year Week Week

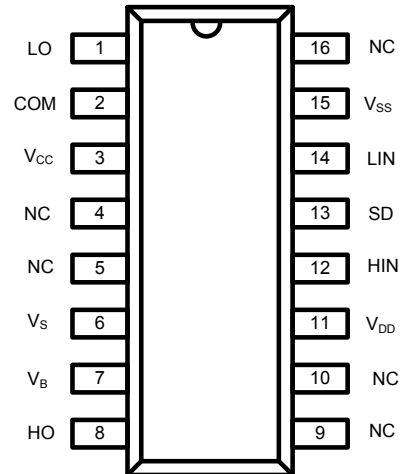
Ordering Information

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2110-3BS	PDIP-14	Tube / 25	YYWW TF2110 Lot ID
TF2110-TEU	SOIC-16W	Tube / 47	
TF2110-TEH	SOIC-16W	T & R / 2500	YYWW TF2113 Lot ID
TF2113-3BS	PDIP-14	Tube / 25	
TF2113-TEU	SOIC-16W	Tube / 47	
TF2113-TEH	SOIC-16W	T & R / 2500	

Pin Diagrams



Top View: PDIP-14
TF2110 / TF2113



Top View: SOIC-16 Wide
TF2110 / TF2113

Pin Descriptions

PIN NAME	PIN DESCRIPTION
V_{DD}	Logic power supply pin.
HIN	Logic input pin for the high side gate driver output. HIN and HO are in phase.
SD	Logic input shutdown pin.
LIN	Logic input pin for the low side gate driver output. LIN and LO are in phase.
V_{SS}	Logic ground pin.
V_B	High side gate driver floating power supply pin.
HO	High side gate driver output pin.
V_S	High side gate driver floating power supply return pin.
V_{CC}	Low side gate driver power supply pin.
LO	Low side gate driver output pin.
COM	Low side gate driver power supply return pin.
NC	"No connect" pin.

High-Side and Low-Side Gate Drivers
Absolute Maximum Ratings (NOTE1)

V_B - High side floating supply voltage (TF2110).....-0.3V to +525V
 V_B - High side floating supply voltage (TF2113).....-0.3V to +625V
 V_S - High side floating supply offset voltage..... V_B -25V to V_B +0.3V
 V_{HO} - High side floating output voltage..... V_S -0.3V to V_B +0.3V
 dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side fixed supply voltage.....-0.3V to +25V
 V_{LO} - Low side output voltage.....-0.3V to V_{CC} +0.3V

V_{DD} - Logic supply voltage.....-0.3V to V_{SS} +25V
 V_{SS} - Logic supply offset voltage..... V_{CC} - 25V to V_{CC} +0.3V
 V_{IN} - Logic input voltage (HIN, LIN and SD).. V_{SS} - 0.3V to V_{DD} +0.3V

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$
 SOIC-16W.....1.25W
 PDIP-14.....1.6W

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SOIC-16W Thermal Resistance (NOTE2)

θ_{JC}45 °C/W
 θ_{JA}90 °C/W

PDIP-14 Thermal Resistance (NOTE2)

θ_{JC}35 °C/W
 θ_{JA}75 °C/W

T_J - Junction operating temperature+150 °C

T_L - Lead temperature (soldering, 10s) +300 °C

T_{stg} - Storage temperature range-55 °C to +150 °C

ESD Susceptibility

HBM (**NOTE3**).....2 kV
 MM (**NOTE4**).....200V
 CDM (**NOTE5**).....1.5 kV

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

NOTE3 Human Body Model, applicable standard JESD22-A114

NOTE4 Machine Model, applicable standard JESD22-A115

NOTE5 Field Induced Charge Device Model, applicable standard JESD22-C101

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 10$		$V_S + 20$	V
V_S	High side floating supply offset voltage	TF2110	Note 6	500	V
		TF2113	Note 6	600	V
V_{HO}	High side floating output voltage	V_S		V_B	V
V_{CC}	Low side fixed supply voltage	10		20	V
V_{LO}	Low side output voltage	0		V_{CC}	V
V_{DD}	Logic supply voltage	$V_{SS} + 3$		$V_{SS} + 20$	V
V_{SS}	Logic supply offset voltage	-5 (Note 7)		5	V
V_{IN}	Logic input voltage (HIN, LIN and SD)	V_{SS}		V_{DD}	V
T_A	Ambient temperature	-40		125	°C

Note 6 Logic operational for $V_S = -4V$ to +500V. Logic state held for $V_S = -4V$ to $-V_{BS}$.

Note 7 When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

DC Electrical Characteristics (NOTE8)

$V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25^\circ C$ and $V_{SS} = COM$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage		9.5			V
V_{IL}	Logic "0" input voltage				6.0	V
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 0A$			1.2	V
V_{OL}	Low level output voltage, V_O	$I_O = 0A$			0.1	V
I_{LK}	Offset supply leakage current	$V_B = V_S = 500V / 600V$			50	μA
I_{BSQ}	Quiescent V_{BS} supply current	$V_{IN} = 0V$ or V_{DD}		125	230	μA
I_{CCQ}	Quiescent V_{CC} supply current	$V_{IN} = 0V$ or V_{DD}		180	340	μA
I_{DDQ}	Quiescent V_{DD} supply current	$V_{IN} = 0V$ or V_{DD}		15	30	μA
I_{IN+}	Logic "1" input bias current	$V_{IN} = V_{DD}$		20	40	μA
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0V$			1	μA
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.5	8.6	9.7	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.0	8.2	9.4	V
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.4	8.5	9.6	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.0	8.2	9.4	V
I_{O+}	Output high short circuit pulsed current	$V_O = 0V, V_{IN} = V_{DD}$ $PW \leq 10 \mu s$	2.0	2.5		A
I_{O-}	Output low short circuit pulsed current	$V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$	2.0	2.5		A

AC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25^\circ C$ and $V_{SS} = COM$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	$V_S = 0V$		120	150	ns
t_{OFF}	Turn-off propagation delay	$V_S = 500V / 600V$		94	125	ns
t_{SD}	Shut-down propagation delay	$V_S = 500V / 600V$		110	140	ns
t_r	Turn-on rise time			25	35	ns
t_f	Turn-off fall time			17	25	ns
t_{DM}	Delay matching	TF2110			10	ns
		TF2113			20	ns

Note 8 The V_{IH} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input pins: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.

Timing Diagram and Waveform Definitions

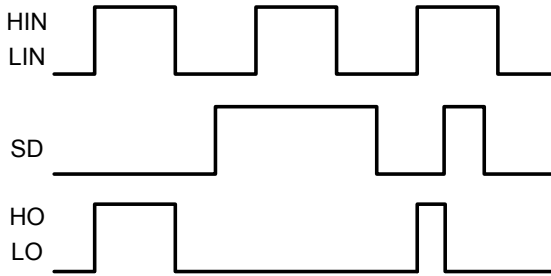


Figure 1. Input / Output Timing Diagram

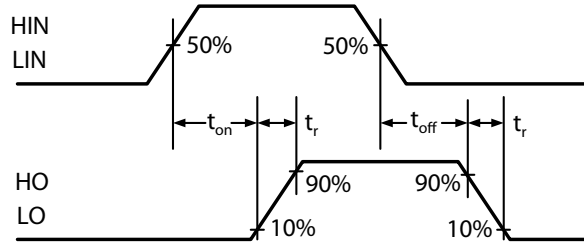


Figure 2. Switching Time Waveform Definition

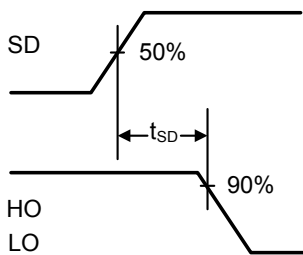


Figure 3. Shutdown Waveform Definitions

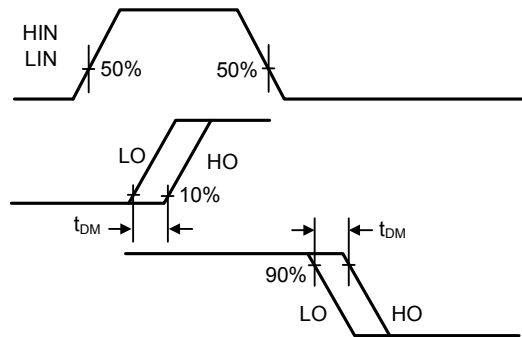
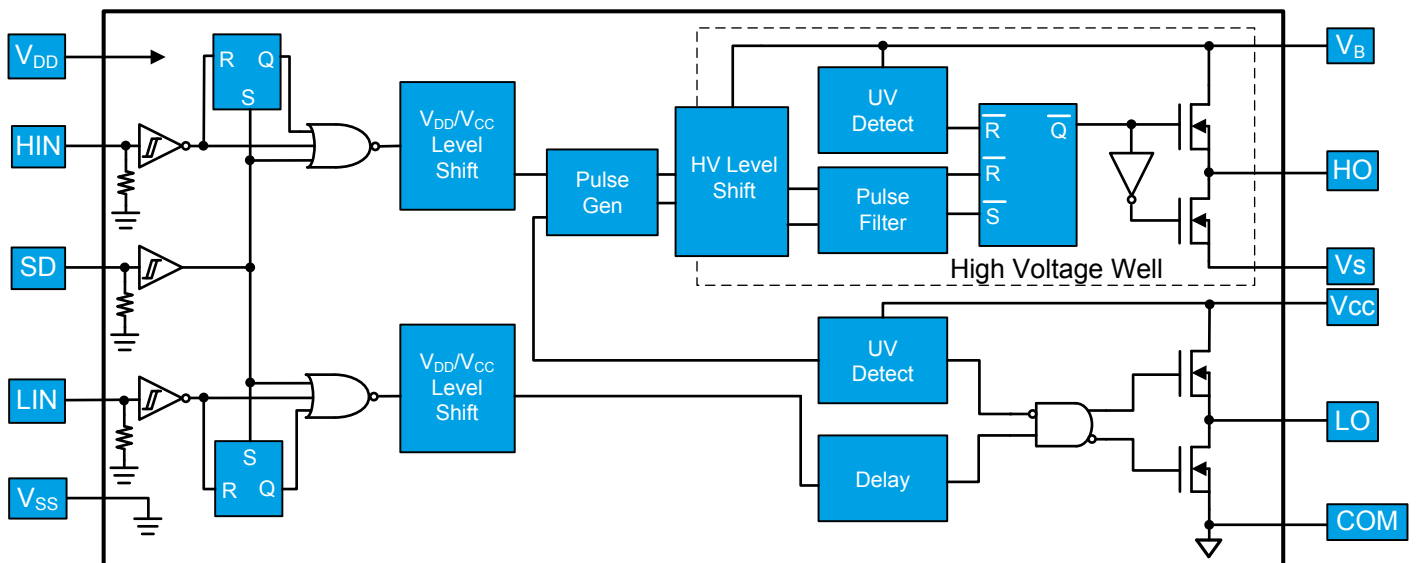


Figure 4. Delay Matching Waveform Definitions

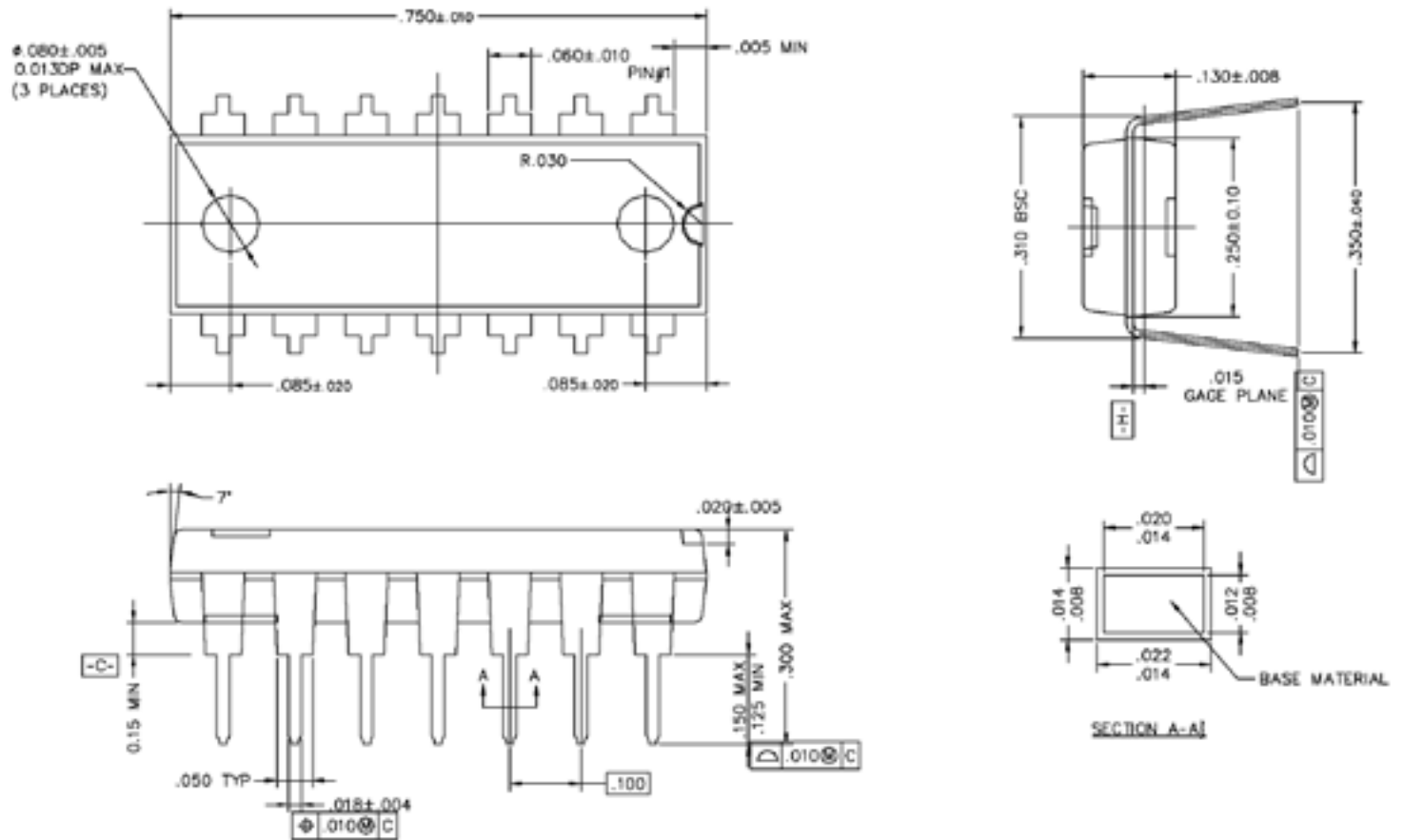
Functional Block Diagram



High-Side and Low-Side Gate Drivers
Package Dimensions (PDIP-14)

Please contact support@telefunkensemi.com for package availability

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

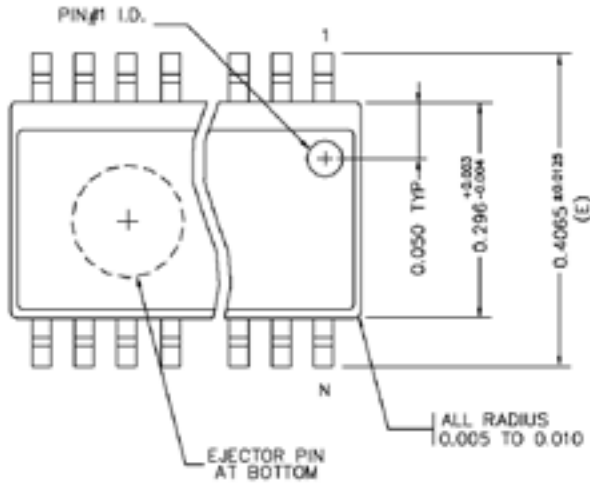


Note: Drawing conforms to jedec ref. MS-001 rev D

Package Dimensions (SOIC-16 W)

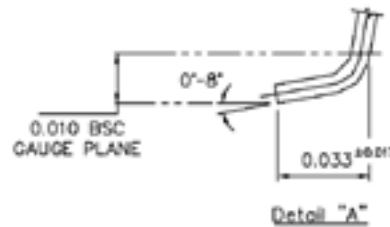
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ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

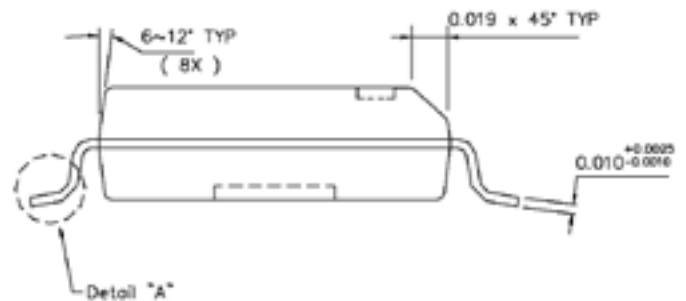
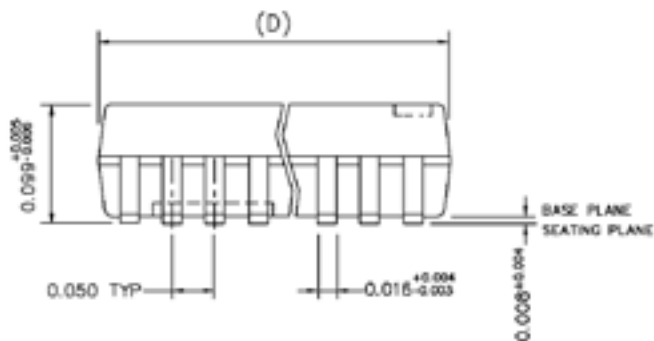


NOTES:

1. "D" AND "L" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.003 INCHES (\perp SEATING PLANE) OUTGOING ASSEMBLY & 0.004 INCHES AFTER TEST.
4. DRAWING CONFORMS TO JEDEC REF. WS-013 REV. E



N	D VARIATIONS		
	MIN	NOM	MAX
16	0.398	0.405	0.412
20	0.496	0.503	0.510
24	0.599	0.606	0.613
28	0.697	0.704	0.711



Notes

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