TELEFUNKEN
Semiconductors

TF12A

Low Power Off-Line SMPS Primary Switcher

Features

- V_{DD} range: 9V to 38V
- 60 kHz fixed frequency operation
- Current-mode control
- Auxiliary under-voltage lockout with hysteresis
- High-voltage start-up current source
- Over-voltage, over-current and over-temperature protection with auto-restart
- Industrial temperature range: -40 °C to +85 °C
- Drop-in replacement for the VIPer12A

Applications

- Switch Mode Power Supplies
- Auxiliary Power Supplies for Industrial Systems
- Adapters for Portable Electronics

Typical Power Capability

MAINS TYPE	PDIP-8	SOIC-8(N)
European (195 - 265 Vac)	13W	8W
Universal (85 - 265 Vac)	8W	5W

Description

The TF12A is a low power primary switcher best suitable for Off-line SMPS battery charger adapters, auxiliary power supplies for industrial systems and standby power supplies for TVs or monitors. It consists of a dedicated current mode PWM controller and a high-voltage Power MOSFET.

The TF12A operates at fixed 60 kHz switching frequency. Its control circuitry provides large V_{DD} range desired in applications in which auxiliary power supply changes are expected. It also provides over-voltage, over-current and over-temperature protection.

The TF12A is offered in 8-pin PDIP and SOIC narrow packages and operates over an extended -40 °C to +85 °C temperature range.

PDIP-8 

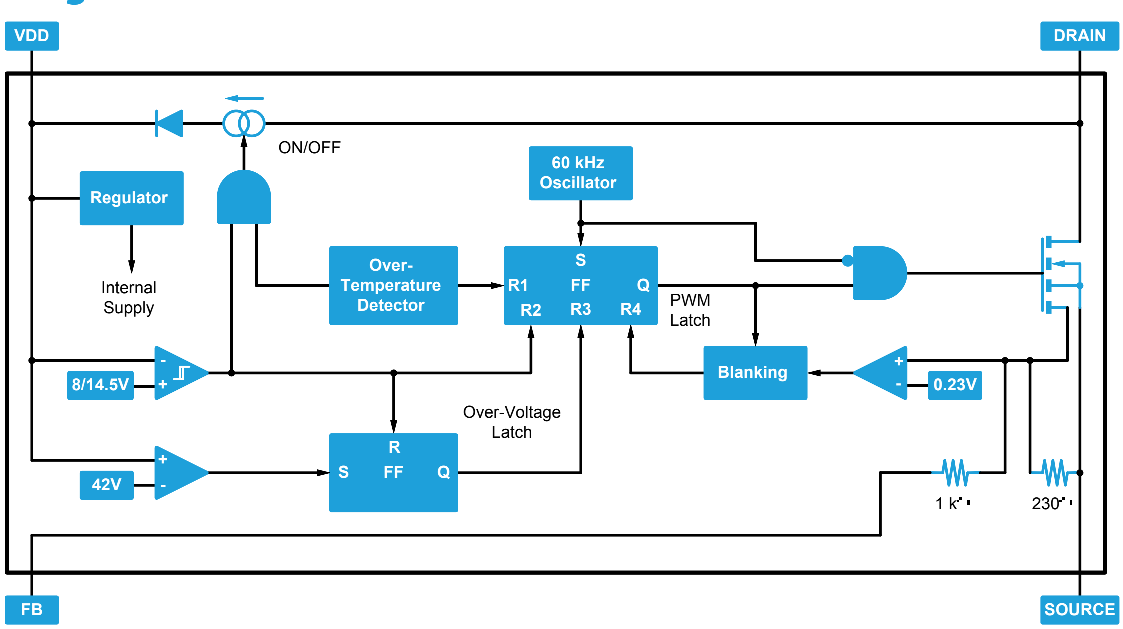
 SOIC-8(N)

Ordering Information

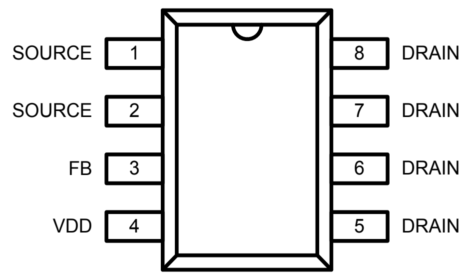
Year Year Week Week

PART NUMBER	PACKAGE	PACKING / Qty	MARK
TF12A-3AS	PDIP-8	Tube, 50	YYWW TF12A Lot ID
TF12A-TAU	SOIC-8(N)	Tube, 95	YYWW TF12A Lot ID
TF12A-TAH	SOIC-8(N)	Tape & Reel, 2500	

Function Diagram



Pin Diagram

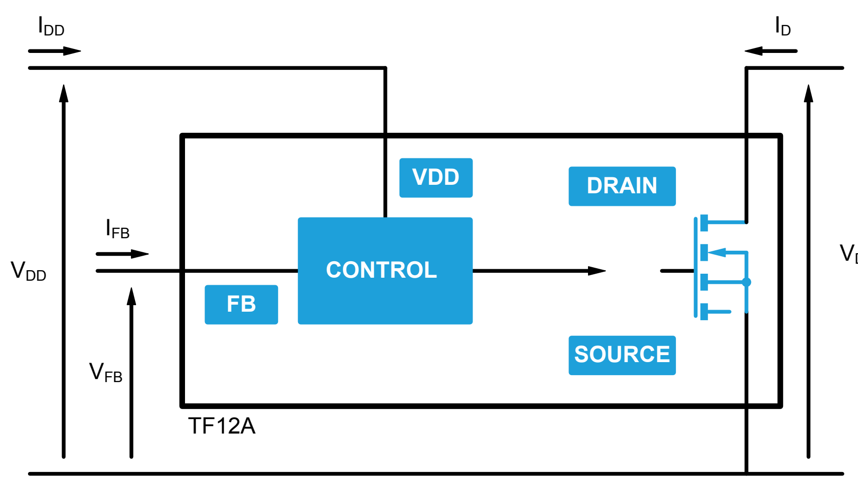


Top View: SOIC-8(N), and PDIP-8

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
V_{DD}	4	Control circuitry power supply pin.
SOURCE	1, 2	Power MOSFET source pin.
DRAIN	5, 6, 7, 8	Power MOSFET drain pin. These 4 pins need to be shorted together on the PC board.
FB	3	Feedback input pin.

Voltage and Current Conventions



Absolute Maximum Ratings *(NOTE1)*

$V_{DS(SW)}$ - Switching drain source voltage ***(NOTE2)*** ......-0.3V to +730V
$V_{DS(ST)}$ - Start-up drain source voltage ***(NOTE3)*** ....-0.3V to +400V
I_D - Continuous drain current ....Internally limited
V_{DD} - Supply voltage ....0V to +50V
I_{FB} - Feedback current ....3 mA

PDIP-8 Thermal Resistance ***(NOTE4)***
θ_{JC}...15 °C/W
θ_{JA}[1]..45 °C/W

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
NOTE2 *This parameter applies when the start-up current is OFF. This is the case when the V_{DD} voltage has reached V_{DDon} and remains above V_{DDoff}.*
NOTE3 *This parameter applies when the start-up current source is ON. This is the case when the V_{DD} voltage has not yet reached V_{DDon} or has fallen below V_{DDoff}.*
NOTE4 *When mounted on a standard 4 layer Jedec board.*

SOIC-8(N) Thermal Resistance ***(NOTE5)***
θ_{JC}...25 °C/W
θ_{JA}...55 °C/W

T_J - Junction operating temperature ....Internally limited
T_C - Case operating temperature range ....-40 °C to +150 °C
T_{stg} - Storage temperature range ....-55 °C to +150 °C

ESD Susceptibility
HBM ***(NOTE6)***...1 kV
CDM ***(NOTE7)***..1.25 kV

NOTE5 *When mounted on a standard 4 layer Jedec board.*
NOTE6 *Human Body Model, applicable standard JESD22-A114-C*
NOTE7 *Field Induced Charge Device Model, applicable standard JESD22-C101-C*

Electrical Characteristics

T_J = 25 °C, V_{DD} = 18V, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Power MOSFET Specifications						
BV_{DSS}	Drain-source voltage	I_D = 1 mA, V_{FB} = 2V	730			V
I_{DSS}	Off State drain current	V_{DS} = 500V, V_{FB} = 2V, T_J = 125 °C			0.1	mA
$R_{DS(ON)}$	Static drain-source On State resistance	I_D = 0.2A I_D = 0.2A, T_J = 125 °C		27	30 54	Ω
t_f	Fall time	I_D = 0.1A, V_{IN} = 300V (***NOTE8***) (See Figures 1 and 2 on page 5)		100		ns
t_r	Rise time	I_D = 0.2A, V_{IN} = 300V (***NOTE8***) (See Figures 1 and 2 on page 5)		50		ns
C_{OSS}	Drain capacitance	V_{DS} = 25V		40		pF

NOTE8 *On clamped inductive load.*

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Control Circuitry Power Supply Specifications						
I_{DDch}	Start-up charging current	V_{DS} = 100V, V_{DD} = 0V-V_{DDon} (See Figure 3 on page 5)		-1		mA
I_{DDoff}	Start-up charging current in thermal shutdown	V_{DS} = 100V, V_{DD} = 5V $T_J > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating supply current not switching	I_{FB} = 2 mA		3	5	mA
I_{DD1}	Operating supply current switching	I_{FB} = 0.5 mA, I_D = 50 mA (***NOTE9***)		4.5		mA
D_{RST}	Restart duty cycle	(See Figure 4 on page 5 and Figure 5 on page 6)		16		%
V_{DDoff}	V_{DD} Undervoltage shutdown threshold	(See Figures 3 and 4 on page 5 and Figure 5 on page 6)	7	8	9	V
V_{DDon}	V_{DD} Startup threshold		13	14.5	16	V
V_{DDhyst}	V_{DD} Threshold hysteresis	(See Figure 3 on page 5)	5.8	6.5	7.2	V
V_{DDovp}	V_{DD} Overvoltage threshold		38	42	46	V
Oscillator Specifications						
f_{OSC}	Oscillator frequency	$V_{DD} = V_{DDoff}$ to 35V, T_J = 0 to 100 °C	54	60	66	kHz
PWM Comparator Specifications						
G_{ID}	I_{FB} to I_D current gain	(See Figures 6,7, and 8 on page 6)		320		
I_{Dlim}	Peak current limitation	V_{FB} = 0V (See Figures 6,7, and 8 on page 6)	0.32	0.4	0.48	A
I_{FBsd}	I_{FB} Shutdown current	(See Figures 6,7, and 8 on page 6)		0.9		mA
R_{FB}	FB Pin input impedance	I_D = 0 mA (See Figures 6,7, and 8 on page 6)		1.2		kΩ
t_d	Current sense delay to turn-OFF	I_D = 0.2A		200		ns
t_b	Blanking time			500		ns
t_{ONmin}	Minimum turn-ON time			700		ns
Over-temperature Circuitry Specifications						
T_{SD}	Thermal shutdown temperature	(See Figure 9 on page 7)	140	170		°C
T_{HYST}	Thermal shutdown hysteresis	(See Figure 9 on page 7)		40		°C

NOTE9 *These test conditions obtained with a resistive load are leading to the maximum conduction time of the device.*

Test Circuits and Timing Diagrams

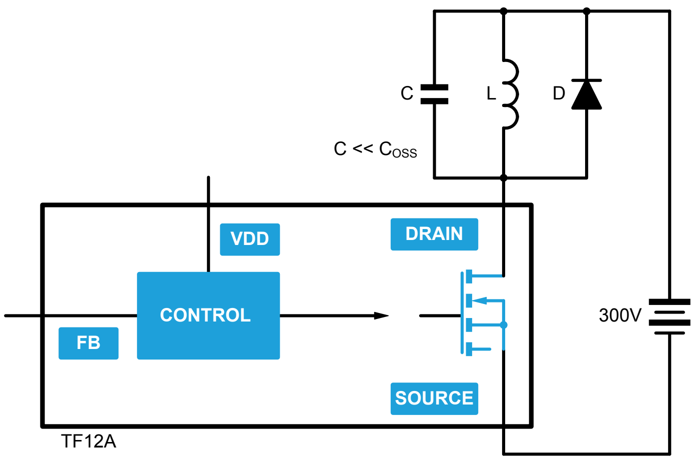


Figure 1. Rise and Fall Time Test Setup

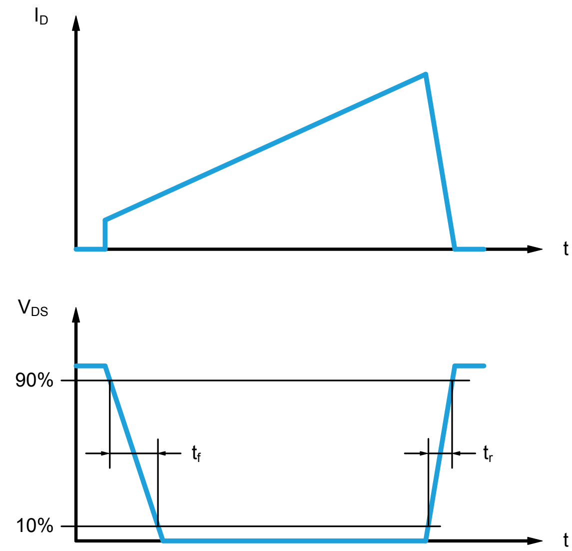


Figure 2. Rise and Fall Time Timing Diagram

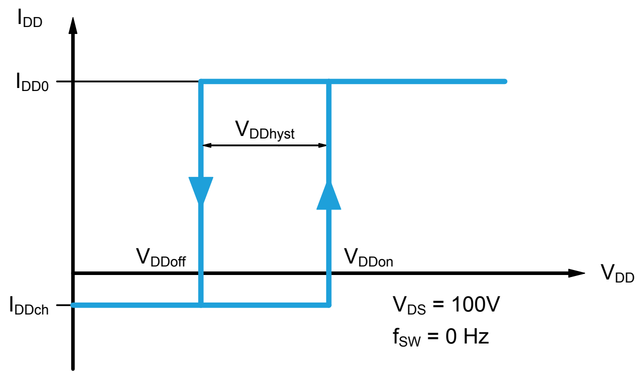


Figure 3. Start-up I_{DD} Current as a Function of V_{DD}

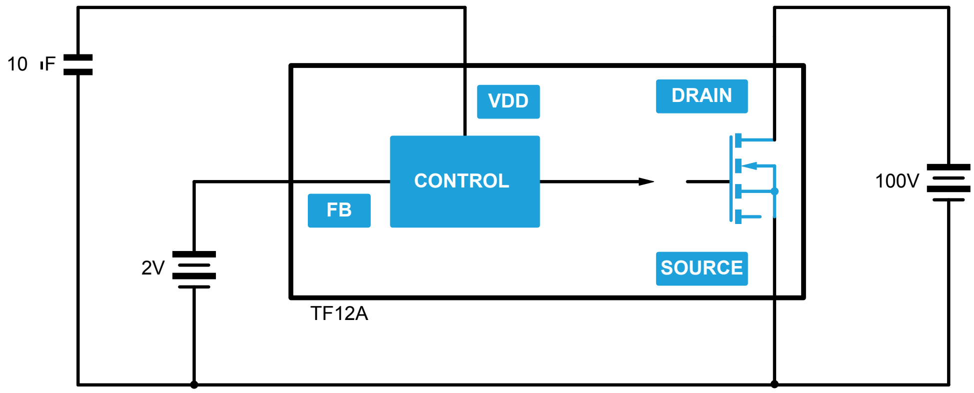


Figure 4. Restart Duty-cycle Test Setup

Test Circuits and Timing Diagrams

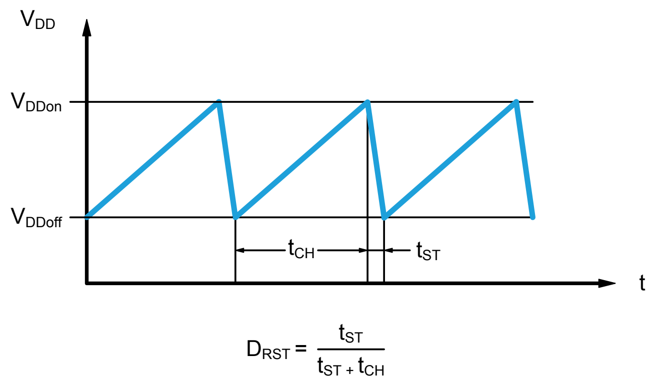


Figure 5. Restart Duty-cycle Timing Diagram

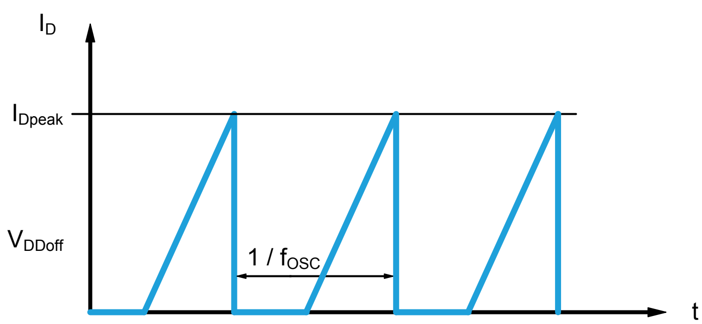
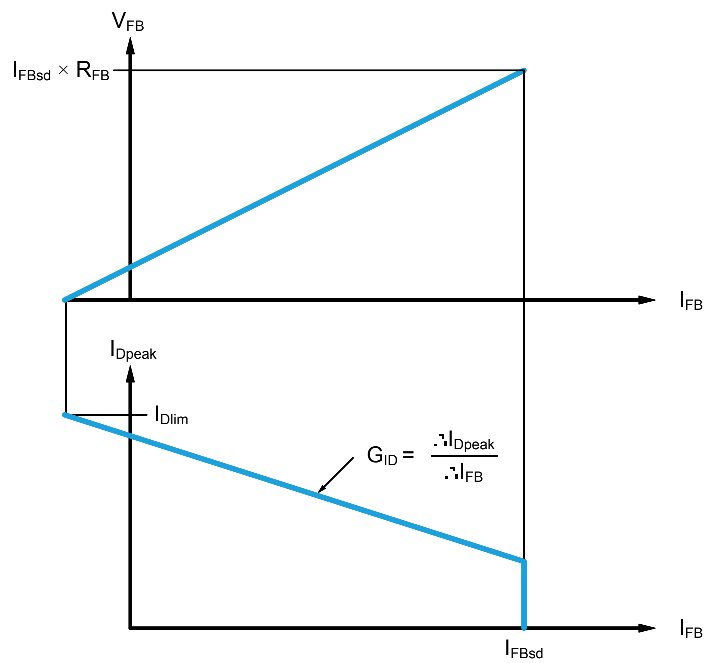


Figure 6. Drain Current Timing Diagram



NOTE: The drain current limitation is obtained for V_{FB} = 0V and a negative current is drawn from the FB pin.

Figure 7. Peak Drain Current vs. Feedback Current

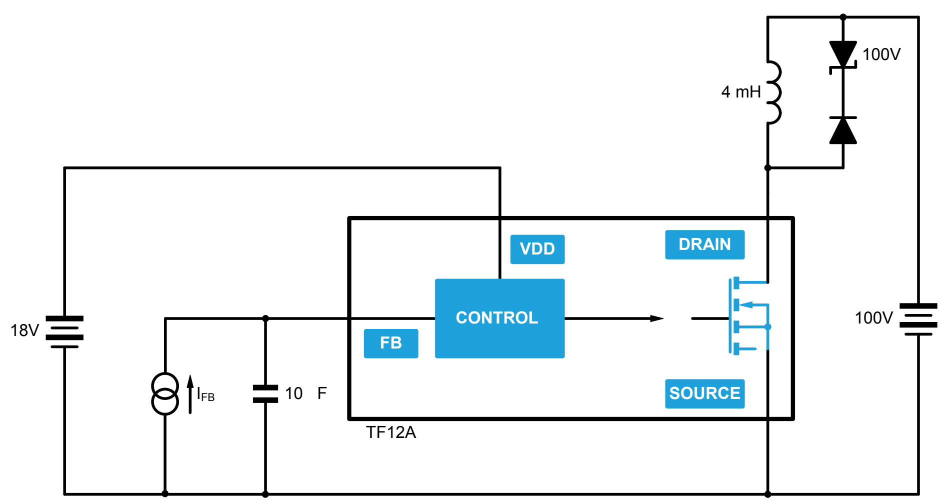


Figure 8. Drain Current and Feedback Current Test Setup

Test Circuits and Timing Diagrams

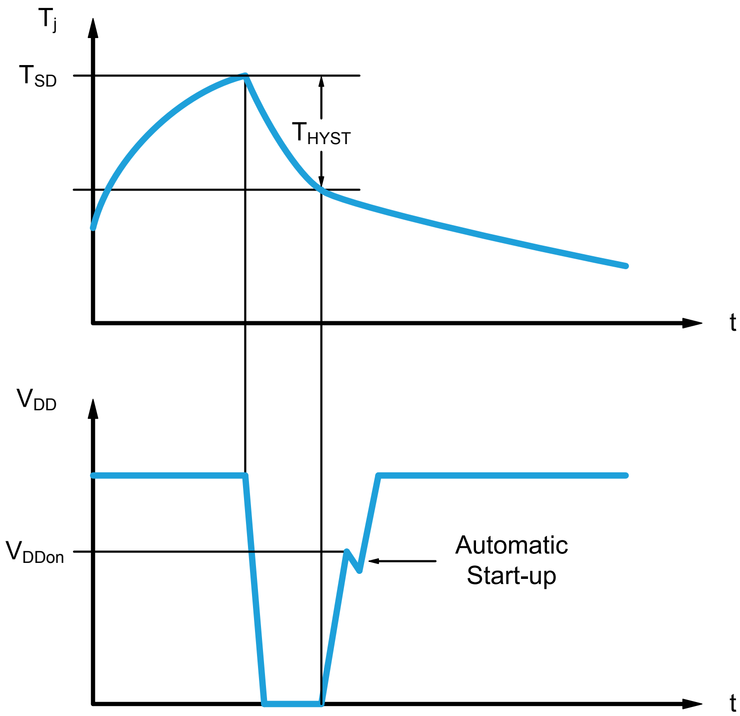


Figure 9. Restart Duty-cycle Timing Diagram

Device Operation

Feedback Pin Principle of Operation

The feedback (FB) pin controls the operation of the device. Unlike conventional PWM control circuits that use a voltage input, the TF12A FB pin is sensitive to current. Figure 10 shows the internal current mode structure of the device.

The power MOSFET delivers a sense current I_S which is proportional to the main current, I_d. The resistor R_2 receives the sum of the currents I_S and I_{FB}. The voltage across R_2 is then compared to the fixed reference voltage of approximately 0.23V. The MOSFET is switched off when the Eq. 1 is reached.

$$R2\,(I_S + I_{FB}) = 0.23V \quad (\textbf{Eq. 1})$$

By extracting I_S, Eq. 2 is obtained:

$$I_S = (0.23V / R_2) - I_{FB} \quad (\textbf{Eq.2})$$

By using the current sense ratio of the MOSFET G_{ID}, Eq. 3 is reached.

$$I_D = G_{ID} \times I_S = G_{ID} \times ((0.23V / R_2) - I_{FB}) \quad (\textbf{Eq.3})$$

The current limitation is obtained with the FB pin shorted to ground (V_{FB} = 0V). This leads to a negative current sourced by the FB pin as expressed in **Eq. 4**

$$I_{FB} = -(0.23V / R_1) \quad (\textbf{Eq. 4})$$

By combining the **Eq. 3** and **Eq. 4**, the expression for the drain current limitation is simply solved and presented in **Eq.5**.

$$I_{Dlim} = G_{ID} \times 0.23V \times (1/R_1 + 1/R_2) \quad (\textbf{Eq. 5})$$

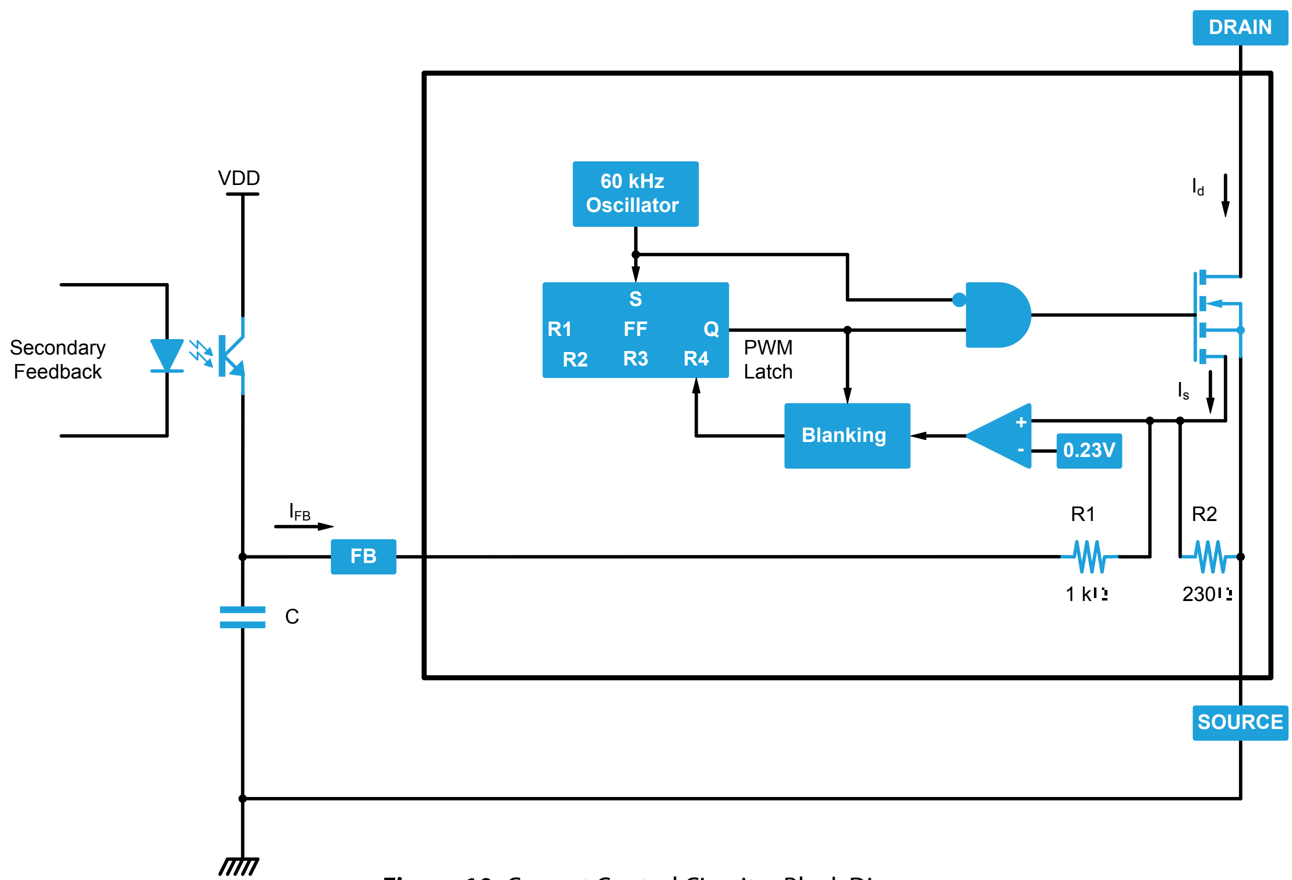


Figure 10. Current Control Circuitry Block Diagram

Device Operation

Feedback Pin Principle of Operation (continued)

In a real application, the FB pin is driven with an optocoupler which acts as a pull up. This is shown in Figure 10. Therefore, it is not possible to short this pin to ground and the drain current value is not achievable. Nevertheless, the capacitor C is averaging the voltage on the FB pin, and when the optocoupler is off (start up or short circuit), it can be assumed that the corresponding voltage is very close to 0V.

For low drain currents, the Eq. 1 is valid as long as $I_{FB} < I_{FBsd}$, where I_{FBsd} is an internal threshold of the TF12A. If I_{FB} exceeds this threshold the device will stop switching. This is represented in Figures 6, 7 and 8, and I_{FBsd} value is specified in the PWM Comparator Specifications section. Actually, as soon as the drain current is about 12% of I_{dlim}, that is to say 85 mA, the device will enter a burst mode operation by missing switching cycles. This is especially important when the converter is lightly loaded.

It is then possible to build the total DC transfer function between I_D and I_{FB} as shown in Figure 11. This figure also takes into account the internal blanking time and its associated minimum turn on time. This imposes a minimum drain current under which the device is no more able to control it in a linear way. This drain current depends on the primary inductance value of the transformer and the input voltage. Two cases may occur, depending on the value of this current versus the fixed 85 mA value, as described above.

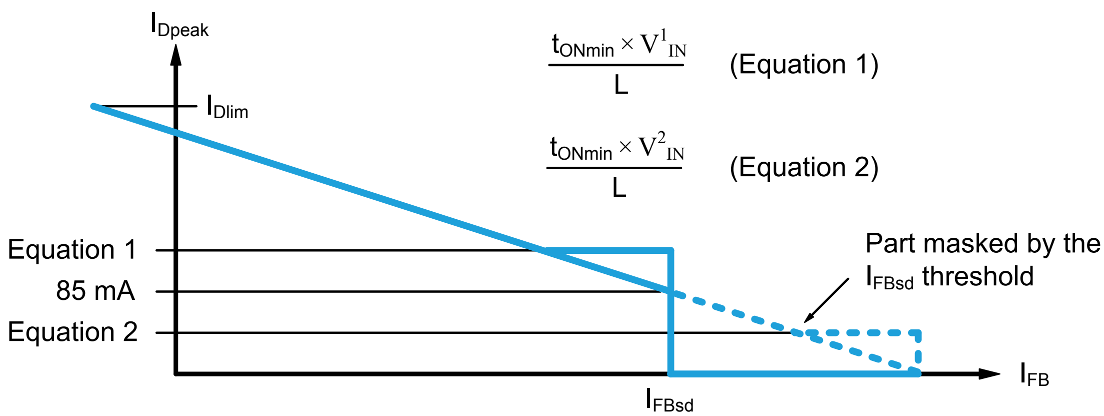


Figure 11. I_{FB} Transfer Function

Device Operation (continued)

Start-up Sequence

This device includes a high voltage start up current source connected on the drain of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated as long as V_{DD} is lower than V_{DDon}. When reaching V_{DDon}, the start up current source is switched OFF and the device begins to operate by turning on and off its main power MOSFET. As the FB pin does not receive any current from the optocoupler, the device operates at full current capacity and the output voltage rises until reaching the regulation point where the secondary loop begins to send a current in the optocoupler. At this point, the converter enters a regulated operation where the FB pin receives the amount of current needed to deliver the right power on secondary side.

This sequence is shown in Figure 12. Note that during the real starting phase t_{ss}, the device consumes some energy from the VDD capacitor, waiting for the auxiliary winding to provide a continuous supply. If the value of this capacitor is too low, the start up phase is terminated before receiving any energy from the auxiliary winding and the converter never starts up. This is illustrated in the same figure in dashed lines.

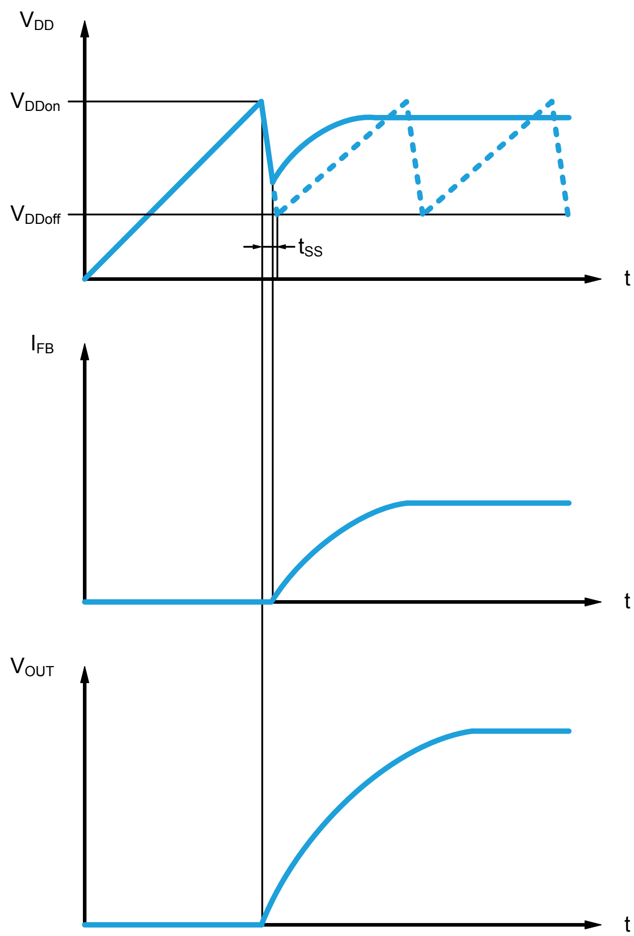


Figure 12. Start-up Sequence

Over-voltage Threshold

An over-voltage detector on the VDD pin allows the TF12A to reset itself when V_{DD} exceeds V_{DDovp}. This is illustrated in Figure 13. which shows the whole sequence of an over-voltage event. Note that this event is only latched for the time needed by V_{DD} to reach V_{DDoff}, and then the device resumes normal operation automatically.

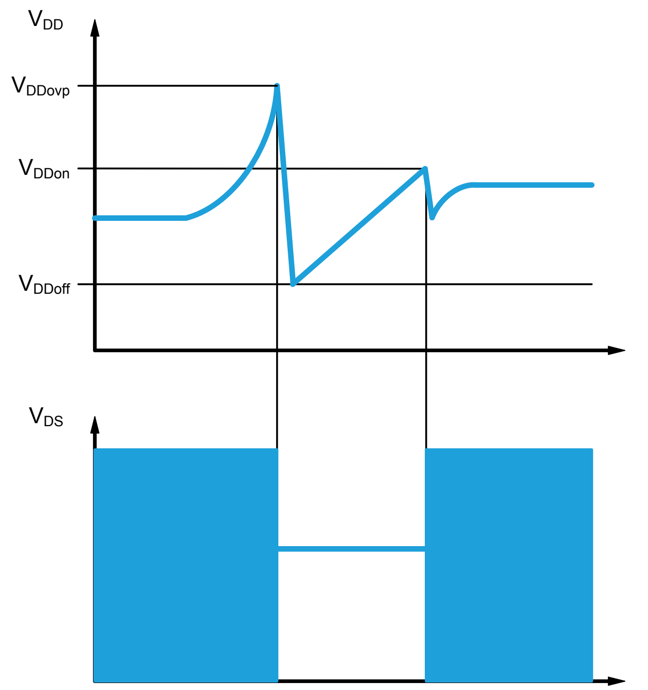
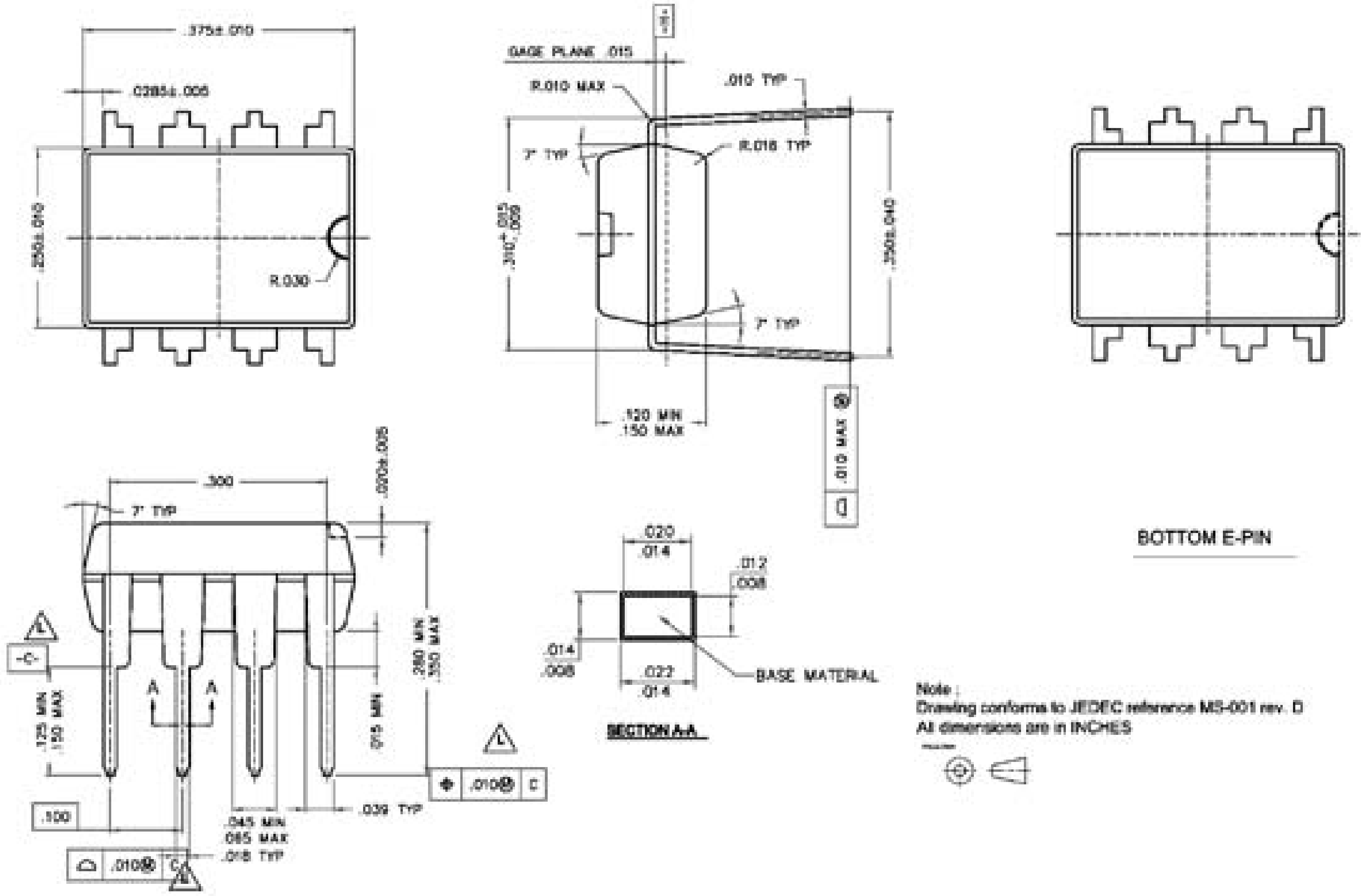


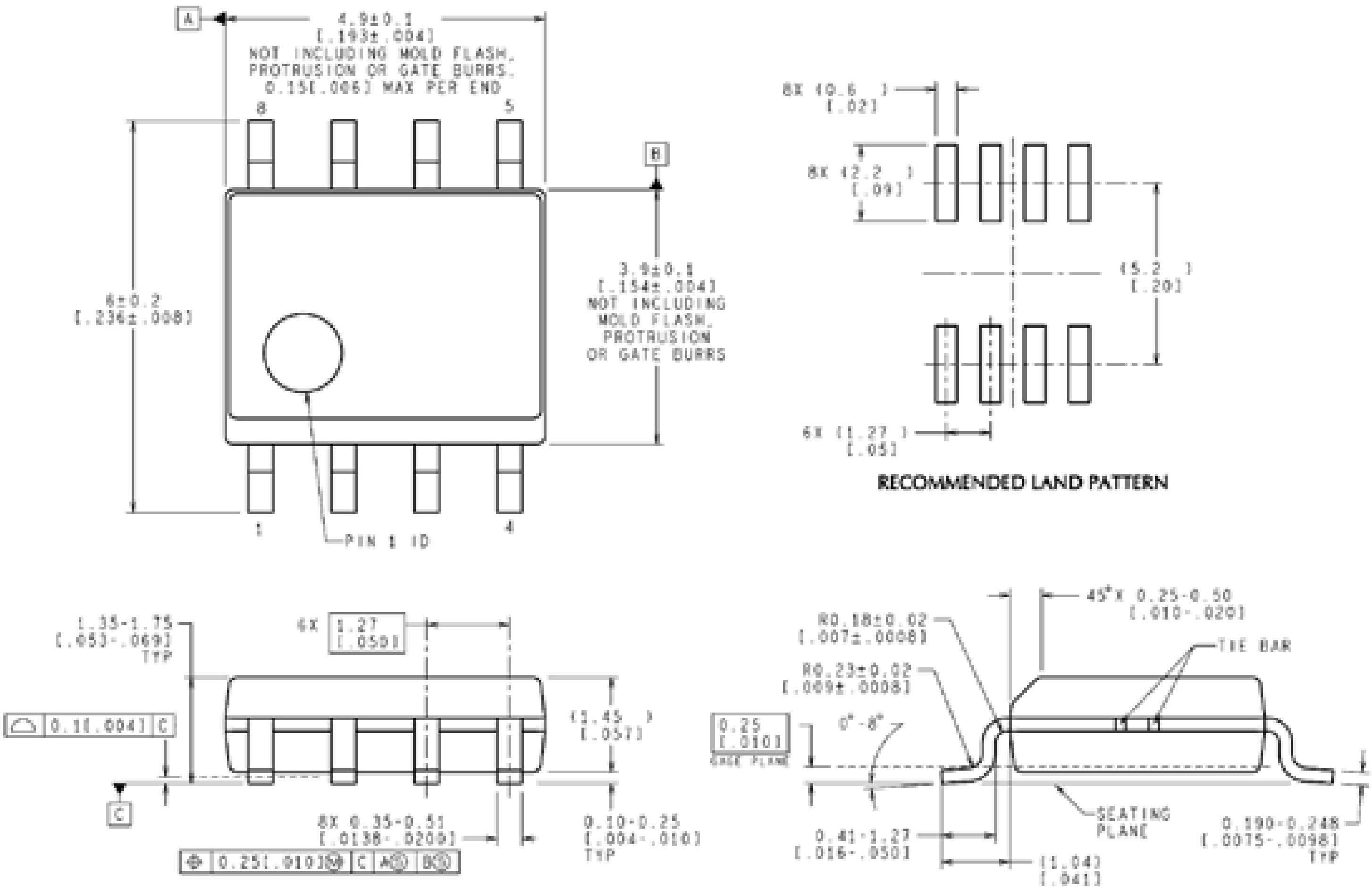
Figure 13. Over-voltage Sequence

Package Dimensions (PDIP-8)



Note :
Drawing conforms to JEDEC reference MS-001 rev. D
All dimensions are in INCHES

Package Dimensions (SOIC-8(N))



NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Notes

Important Notice

For additional information please contact support@telefunkensemi.com or visit www.telefunkensemiconductors.com