TELEFUNKEN
Semiconductors

TF10CP02 / TF10CP22

1.5 Gbps 2x2 LVDS Crosspoint Switches

Features

- **DC to 1.5 Gbps low jitter, low skew, low power operation**
- **Pin configurable, fully differential, non-blocking architecture eases system design and PCB layout**
- **On-chip 100Ω input termination minimizes return loss, component count and board space (TF10CP02 only)**
- **Splitter, mux, repeater or crosspoint**
- **Receivers with wide input voltage range allow easy AC or DC coupled interface to most differential drivers (LVDS, LVPECL, CML)**
- **Point to point applications**
- **Guaranteed operation within industrial temperature range -40° to +85°C**
- **Available in space saving SOIC-16 package**
- **Pin and function compatable with DS90CP22 and SN6SLVCP22**

Applications

- High-Speed Backplane Redundancy
- Wireless Base Stations
- Telecom / Datacom
- Network Routing

Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF10CP02-TBS	SOIC-16(N)	Tube / 48	YYWW TF10CP02TB Lot ID
TF10CP02-TBP		T&R / 500	
TF10CP22-TBS	SOIC-16(N)	Tube / 48	YYWW TF10CP22TB Lot ID
TF10CP22-TBP		T&R / 500	
TF10CP02-6CX	TSSOP-16	Check for Availabilty	YYWW TF10CP026C Lot ID
TF10CP22-6CX	TSSOP-16	Check for Availabilty	YYWW TF10CP226C Lot ID

Replace X *with* U *(Qty = 94) or* G *(Qty = 100).*

TF10CP02 *is Terminated.* TF10CP22 *is* ***Not*** *Terminated.*

Description

The TF10CP02 and TF10CP22 are low-jitter, fully differential, non-blocking LVDS 2x2 crosspoint switches ideal for applications that require high-speed data or clock distribution, switching, buffering, muxing or routing while minimizing power, space, and noise.

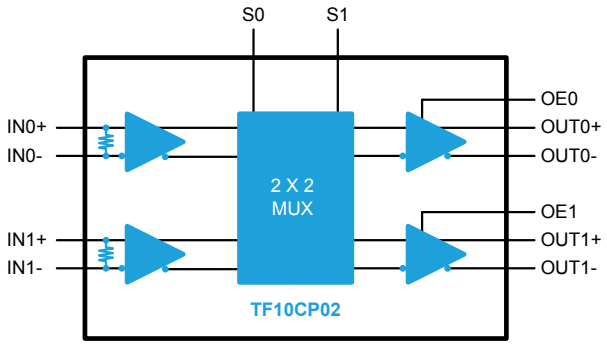
Low 100 ps (max) channel-channel skew and 80 ps P-P (max) added deterministic jitter ensure reliable communication in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery or serializers and deserializers.

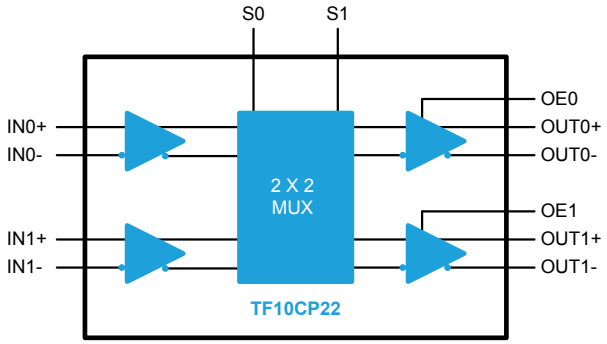
The TF10CP02 features on-chip 100Ω input termination which minimizes input return loss, component count and board space. The TF10CP22 differential inputs are without input termination resistors and are suitable for applications requiring custom termination schemes.

Supply current is 70 mA (max). LVDS inputs and outputs conform to the ANSI/EIA/TIA-644-A standard. The TF10CP02 and TF10CP22 are offered in 16-pin SOIC narrow and TSSOP packages, and operate over an extended -40 °C to +85 °C temperature range.

SOIC-16(N)   TSSOP-16

Function Diagram





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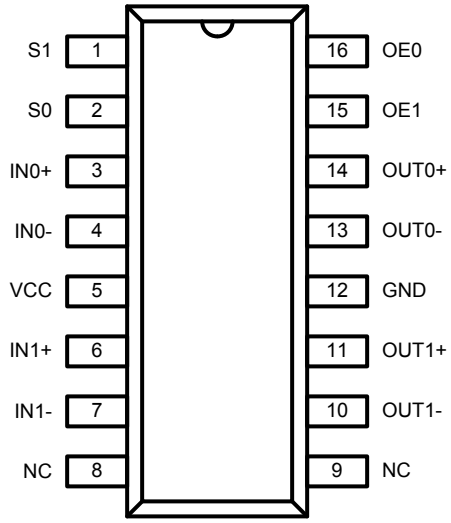
Pin Diagram



Logic Tables

S1	S0	OUT1	OUT0
0	0	IN0	IN0
0	1	IN0	IN1
1	0	IN1	IN0
1	1	IN1	IN1

Table 1. Switch Configuration Truth Table

OE1	OE0	OUT1	OUT0
0	0	Disabled	Disabled
0	1	Disabled	Enabled
1	0	Enabled	Disabled
1	1	Enabled	Enabled

Table 2. Output Enable Truth Table

NOTE *Asserting the OE pin will force zero Volts differential on the disabled output. In the event that downstream devices require a floating output, then AC coupling the outputs is recommended.*

Pin Descriptions

PIN NAME	PIN NUMBER	PIN TYPE	PIN DESCRIPTION
IN0+, IN0-, IN1+, IN1-	3, 4, 6, 7	LVDS inputs	Non-inverting and inverting LVDS input pins.
OUT0+, OUT0-, OUT1+, OUT1-	14, 13, 11, 10	LVDS outputs	Non-inverting and inverting LVDS output pins.
OE0, OE1	16, 15	LVCMOS inputs	Output enable pins.
S0, S1	2, 1	LVCMOS inputs	Switch configuration pins.
VCC	5	Power	Power supply pin.
GND	12	Power	Ground or circuit common pin.
NC	8, 9	NC	“No connect” pins.

Absolute Maximum Ratings[1]

VCC to GND.....-0.5V to +4V

Inputs
- IN+, IN- to GND.....-0.5V to +4V
- OE, S to GND .....-0.5V to +4V
- V_{ID} Differential input voltage 1.2V

Outputs
- OUT+, OUT- to GND.....-0.5V to +4V

Maximum Package Power Dissipation (T_A = +25 °C)
- SOIC-16 (derate 13.8 mW/°C above +25 °C).....1.7 W
- TSSOP-16 (derate 9.7 mW/°C above +25 °C).....1.2W

SOIC-16 Thermal Resistance
- θ_{JC}.....41 °C/W
- θ_{JA}.....72 °C/W

TSSOP-16 Thermal Resistance
- θ_{JC}.....29 °C/W
- θ_{JA}.....103 °C/W

Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 4s) .....+260°C

ESD Susceptibility
- HBM[1].....5 kV
- MM[2].....250V
- CDM[3].....1250V

1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1 Human Body Model, applicable standard JESD22-A114-C
2 Machine Model, applicable standard JESD22-A115-A
3 Field Induced Charge Device Model, applicable standard JESD22-C101-C

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply Voltage	VCC	3	3.3	3.6	V
V_{ID}	Differential input voltage	IN+, IN-	0.1	0.35	1	V
V_{IN}	Input voltage	IN+, IN-	0		V_{CC}	V
V_{IH}	High-level input voltage	OE, S	2		V_{CC}	V
V_{IL}	Low-level input voltage	OE, S	0		0.8	V
T_A	Operating free-air temperature	All	-40	25	85	°C

Electrical Characteristics

Over recommended operating conditions (NOTE1), unless otherwise specified. Typical values are V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Specifications (OE, S pins)						
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH} S	High-level input current	V_{CC} = 3.6V V_{IN} = 3.6V	50	150	225	µA
I_{IH} OE	High-level input current		100	285	450	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V V_{IN} = 0V	-10	0	10	µA
V_{CL}	Input clamp voltage (Note 2)	I_{CL} = -18 mA, V_{CC} = 0V	-1.5	-0.9		V
LVDS Input Specifications (IN+, IN- pins)						
V_{TH}	Differential input high threshold	V_{ICM} = 0.05V or V_{CC} -0.05V		0	100	mV
V_{TL}	Differential input low threshold		-100	0		mV
V_{ID}	Differential input voltage		0.1	0.35	1	V
V_{ICMR}	Input common mode voltage range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input current CP22 (Note 3)	V_{CC} = 3.6V V_{IN} = 0 or 3.6V	-10	+/- 6	10	µA
	Input current CP02 (Note 3)	V_{CC} = 3.6V V_{IN} = 0 or 3.6V	-20	+/-12	20	µA
C_{IN}	Input capacitance	IN+ or IN- to GND		5		pF
R_{IN}	Input termination resistor (TF10CP02 only)	Between IN+ and IN-		100		Ω

NOTE1 *Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.*

NOTE2 *This specification is not production tested and is guaranteed by design simulations.*

NOTE3 *Other input floating or observing the Absolute Maximum Differential input voltage.*

Electrical Characteristics (continued)

Over recommended operating conditions (NOTE1), unless otherwise specified. Typical values are V_{CC} = 3.3V, T_A = 25 °C.

LVDS Output Specifications (OUT+, OUT- pins)						
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 1 R_L = 100Ω	250	370	475	mV
$\|\Delta V_{OD}\|$	Change in magnitude of V_{OD} for complimentary output states		-35		35	mV
$V_{OCM(ss)}$	Steady-state output common mode voltage		1.05	1.35	1.55	mV
$\Delta V_{OCM(SS)}$	Change in magnitude of $V_{OCM(ss)}$ for complimentary output states		-35		35	mV
I_{OS}	Output short circuit current	OUT+ or OUT- to GND		-70	-100	mA
		OUT+ or OUT- to V_{CC}		5	10	
I_{OSD}	Differential output short circuit current	OUT+ and OUT- to GND		-115	-200	mA
		OUT+ and OUT- to V_{CC}		9	20	
C_{OUT}	Output capacitance	OUT+ or OUT- to GND		3.3		pF
Power Supply Current Specifications						
I_{CC}	Power supply current	OE = 1, S1 = 0, S2 = 1		50	70	mA

Switching Characteristics

Over recommended operating conditions (NOTE1), unless otherwise specified. Typical values are V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications (NOTE2)						
t_{PLH}	Propagation delay, low-to-high	See Figures 2, 3 R_L = 100Ω	300	470	750	ps
t_{PHL}	Propagation delay, high-to-low		300	470	750	ps
t_r	Rise time		100	175	400	ps
t_f	Fall time		100	175	400	ps
$t_{SK(p)}$	Pulse skew (NOTE3)			10	75	ps
$t_{SK(c-c)}$	Channel-to-channel skew (NOTE4)			12	100	ps
$t_{SK(p-p)}$	Part-to-part skew (NOTE5)				450	ps
t_{ON}	Propagation delay, OE to On	See Figures 4		8.5	15	ns
t_{OFF}	Propagation delay, OE to Off			6.5	15	ns
t_{SEL}	Select time (NOTE6)			9	20	ns
T_{DJ}	Deterministic Jitter Peak-to-Peak	V_{ID} = 400mV V_{CM} = 1.2V PRBS-7 (NRZ)	622 Mbps	20	70	ps
			1.06 Gbps	20	70	ps
			1.5 Gbps	30	80	ps

NOTE1 *Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.*

NOTE2 *Specification is guaranteed by characterization and is not tested in production.*

NOTE3 *$t_{SK(p)}$, pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).*

NOTE4 *$t_{SK(c-c)}$, channel-to-channel skew, is the difference in propagation delay time (t_{PLH} or t_{PHL}) between both output channels in broadcast mode on the same device at any operating temperature and supply voltage within the recommended operating range.*

NOTE5 *$t_{SK(p-p)}$ part-to-part skew, is defined as the difference between the minimum and maximum differential propagation delay times. It applies to devices operating at the same power supply voltage and within 5°C of each other within the operating temperature range.*

NOTE6 *The state of the outputs is not valid for the duration of the t_{SEL} maximum propagation delay time.*

Test Circuits and Timing Diagrams

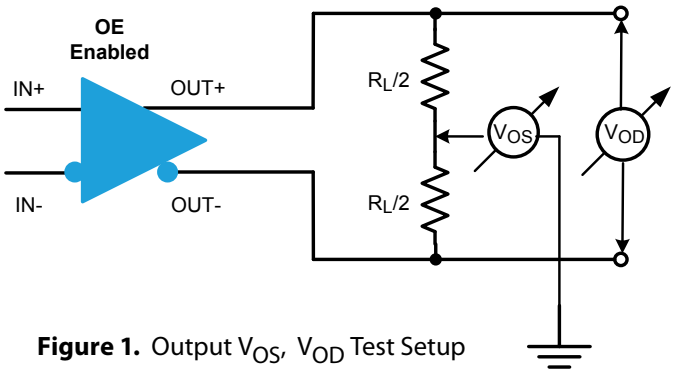
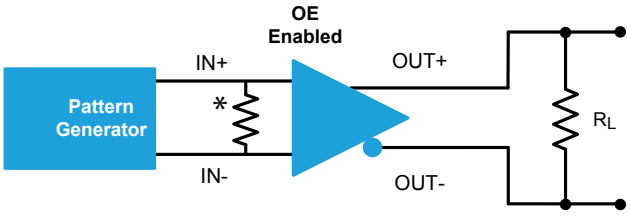


Figure 1. Output V_{OS}, V_{OD} Test Setup



*R_{TERM} = 100Ω, not required for TF10CP02

Figure 2. Propagation Delay and Transition Time Test Setup

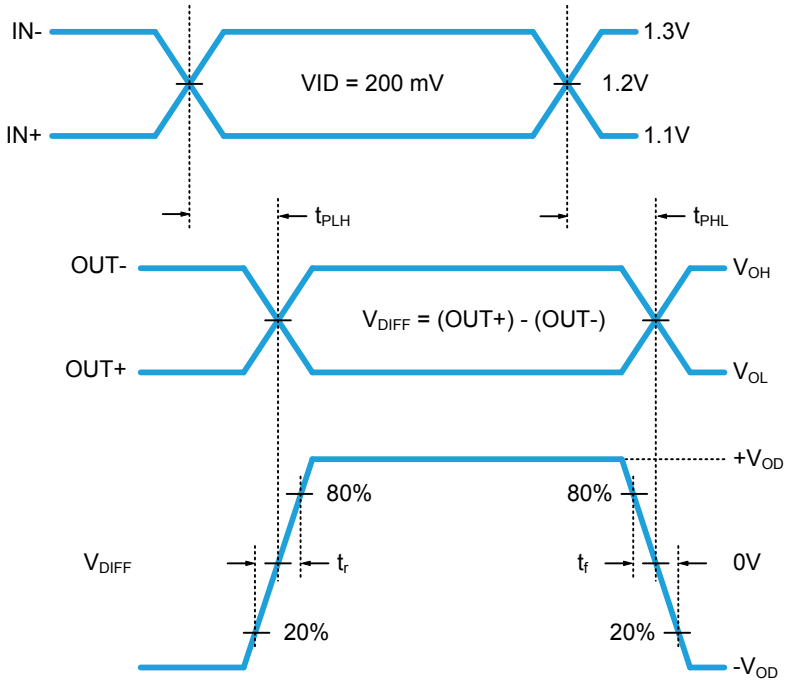


Figure 3. Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams (continued)

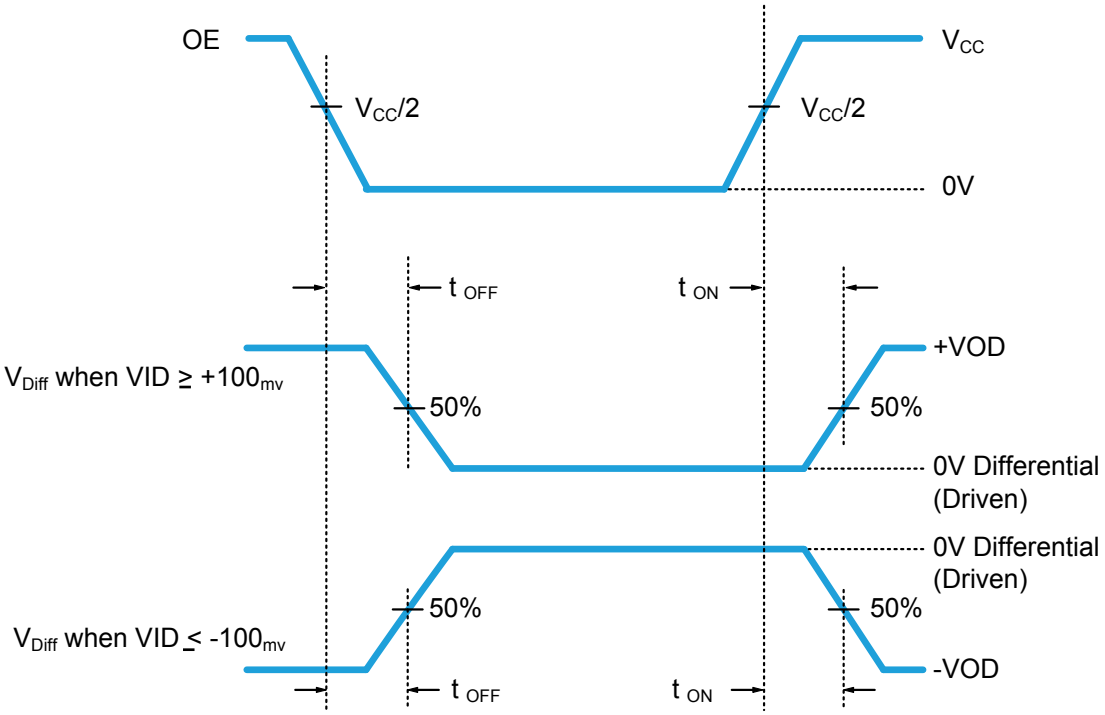
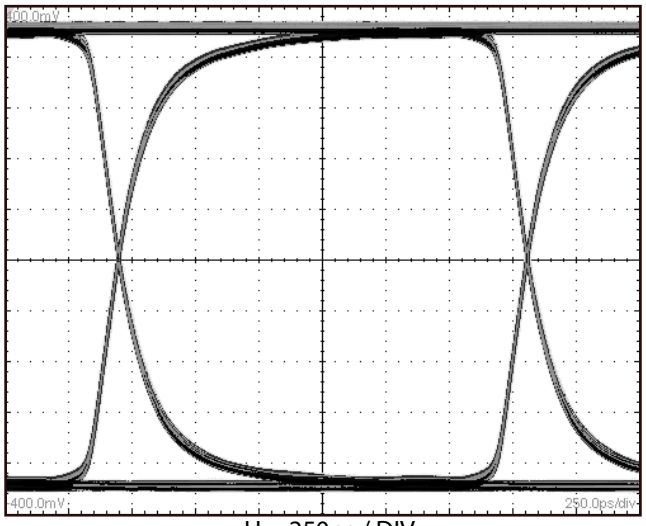


Figure 4. t_{ON} / t_{OFF} Delay Waveforms

Typical Performance Characteristics

V = 80 mV / DIV

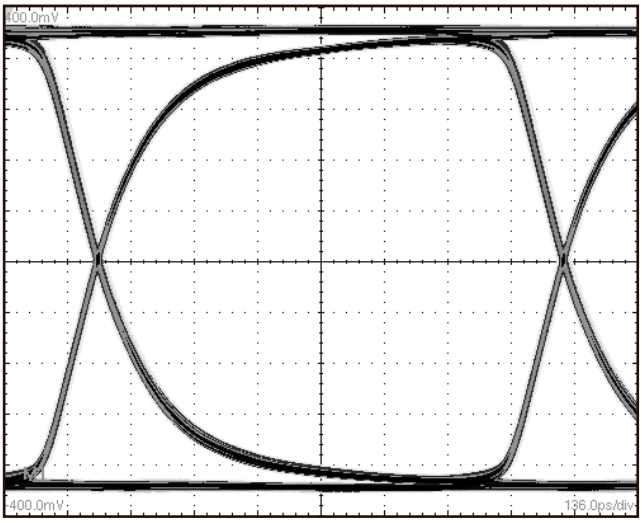
622Mbps NRZ PRBS-7, after 4" of FR-4 stripline, +25°C, 3.3V Vcc.



H = 250ps / DIV

V = 80 mV / DIV

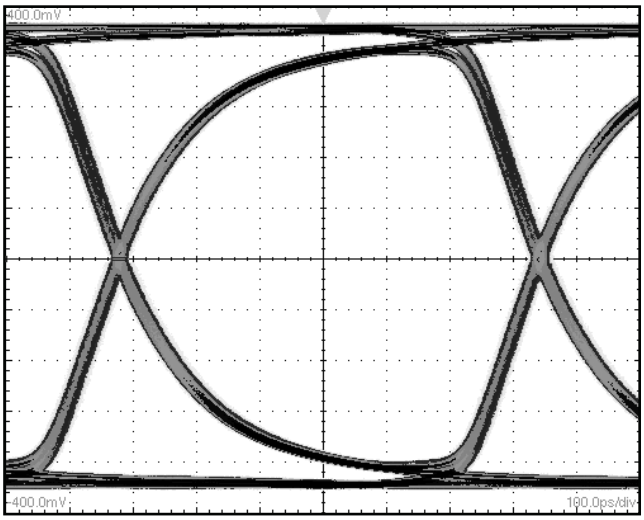
1.06Gbps NRZ PRBS-7, after 4" of FR-4 stripline, +25°C, 3.3V Vcc.



H = 136ps / DIV

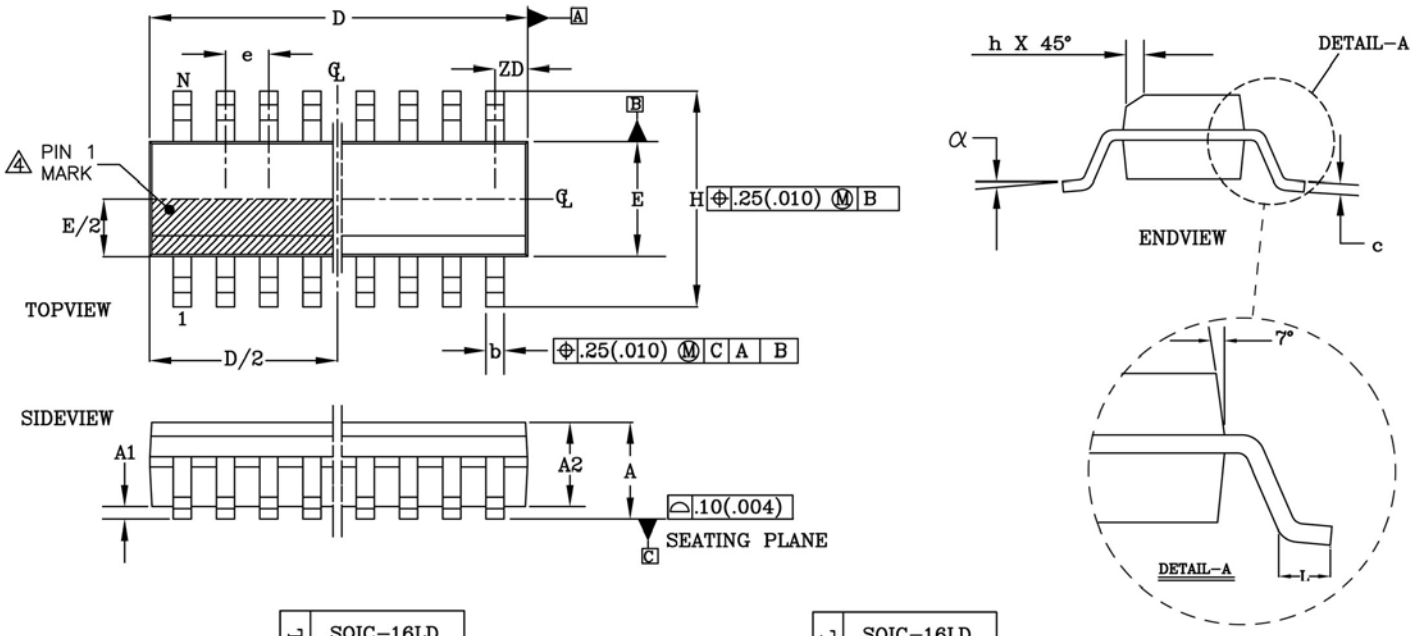
V = 80 mV / DIV

1.5Gbps NRZ PRBS-7, after 4" of FR-4 stripline, +25°C, 3.3V Vcc.



H = 100ps / DIV

Package Dimensions (SOIC-16)



SYMBOL	SOIC–16LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51 REF	
A2	1.37	1.57

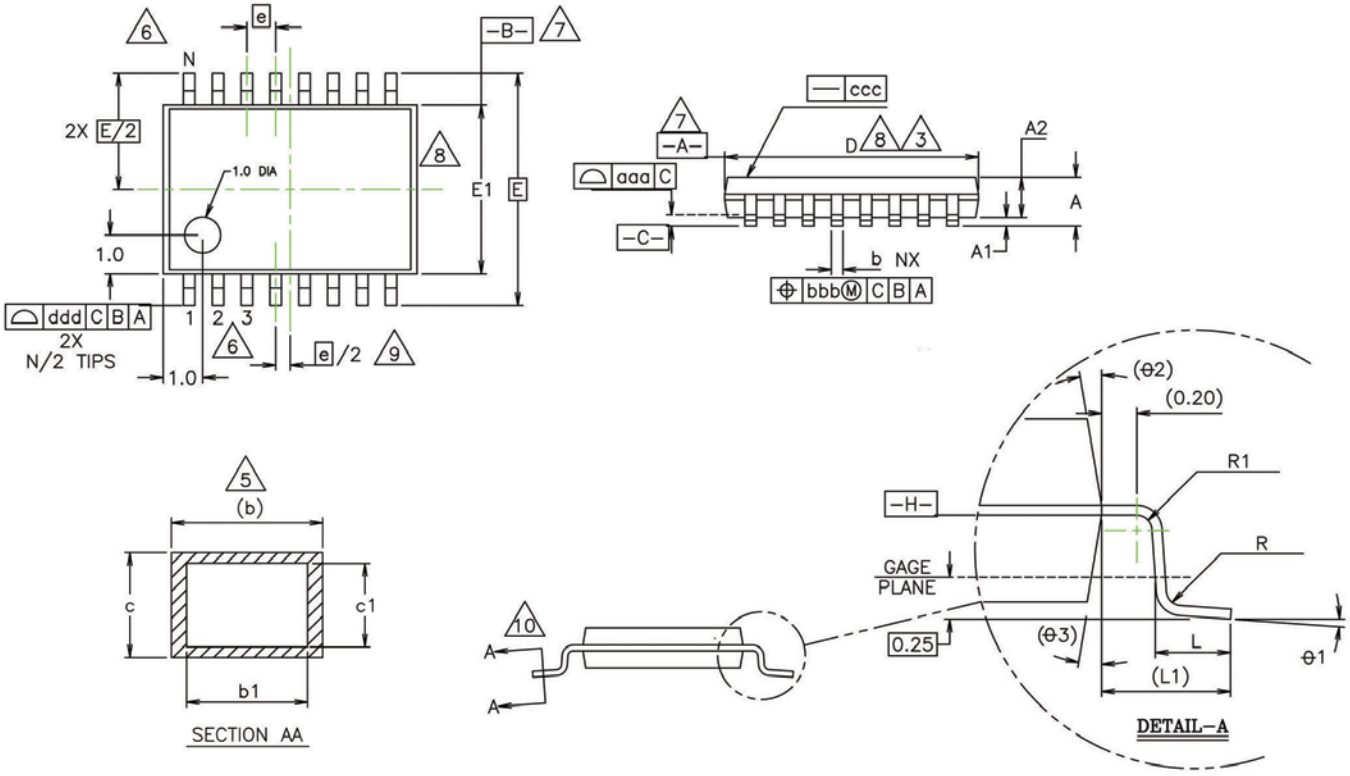
SYMBOL	SOIC–16LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

4 DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

Package Dimensions (TSSOP-16 Please contact support@telekenfunsemi.com for availability)



	0.65mm LEAD PITCH			NOTE
	MIN	NOM	MAX	
A	---	---	1.10	---
A1	0.05	---	0.15	---
A2	0.85	0.90	0.95	---
L	0.50	0.60	0.75	---
R	0.09	---	---	---
R1	0.09	---	---	---
b	0.19	---	0.30	*5*
b1	0.19	0.22	0.25	---
c	0.09	---	0.20	---
c1	0.09	---	0.16	---
θ1	0°	---	8°	---
L1	1.0 REF			---
aaa	0.10			---
bbb	0.10			---
ccc	0.05			---
ddd	0.20			---
e	0.65 BSC			---
θ2	12° REF			---
θ3	12° REF			---
NOTE	*1,2*			

D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	16		

NOTES:

1 ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2 DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3 DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5 DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM FOR 0.5 MM PITCH PACKAGES.

6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

8 DIMENSIONS 'D' AND 'E1' ARE TO BE DETERMINED AT DATUM PLANE -H-.

9 THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE. FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE, DATUM A.

10 CROSS SECTION A–A TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEADTIP.

11 THIS VARIATION IS NOT REGISTERED WITH JEDEC.

12 PACKAGE SURFACE FINISHING:
(I) TOP: MATTE (CHARMILLES: #18~30)
(II) BOTTOM: MATTE (CHARMILLES: #12~27)

Notes

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