TELEFUNKEN
Semiconductors

TF90LVDS032 / TF90LVDT032

Quad LVDS Line Receivers with Extended Common Mode

Features

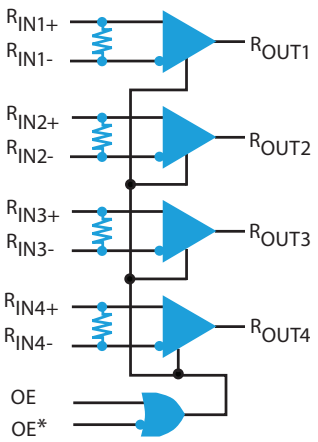
- **Extended input common mode voltage range: -7V to 12V**
- **DC to 400 Mbps / 200 MHz low noise, low skew, low power operation**
  - **—400 ps (max) channel-to-channel skew**
  - **—300 ps (max) pulse skew**
  - **—7 mA (max) power supply current**
- **On-chip 100Ω input termination minimizes return loss, component count and board space (TF90LVDT032 only)**
- **Open or undriven fail-safe support (TF90LVDS032)**
- **LVDS inputs conform to TIA/EIA-644-A standard**
- **Standard output enable scheme eliminates power consumption when device is not in use**
- **Guaranteed operation within industrial temperature range-40° to +85°C**
- **Available in space saving SOIC-16 and TSSOP-16 packages**
- **Pin and function compatible with DS90LV032A and SN65LVDS32 and SN65LVDS32B**

Applications

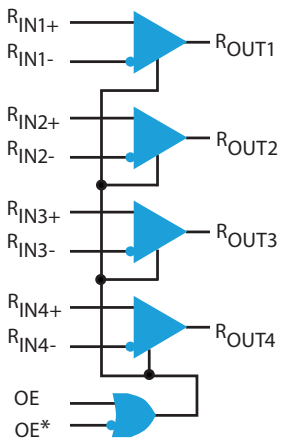
- Digital Copiers
- Wireless Base Stations
- Telecom / Datacom
- Network Routing
- Laser Printers
- LCD Displays

Function Diagrams

TF90LVDT032



TF90LVDS032



Description

The TF90LVDS032 and TF90LVDT032 are 400 Mbps Quad LVDS (low voltage differential signaling) Line Receivers optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e.g. cables, printed circuit board traces, backplanes).

The TF90LVDS032 and TF90LVDT032 accept four LVDS signals and translates them to four LVCMOS signals. Their outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

The TF90LVDS032 and TF90LVDT032 input receivers support wide input voltage range of -7 V to 12 V for exceptional noise immunity. A fail-safe feature sets the outputs to a high state when both inputs are open, or undriven.

The TF90LVDT032 features on-chip 100Ω input termination resistors that minimize input return loss, component count and board space. The TF90LVDS032 differential inputs are without input termination resistors and are suitable for applications requiring custom termination schemes.

Supply current is 7 mA (max). LVDS inputs conform to the ANSI/EIA/TIA-644-A standard. The TF90LVDS032 and TF90LVDT032 are offered in 16-pin SOIC(N) and TSSOP packages and operate over an extended -40 °C to +85 °C temperature range.

SOIC-16(N)

TSSOP-16

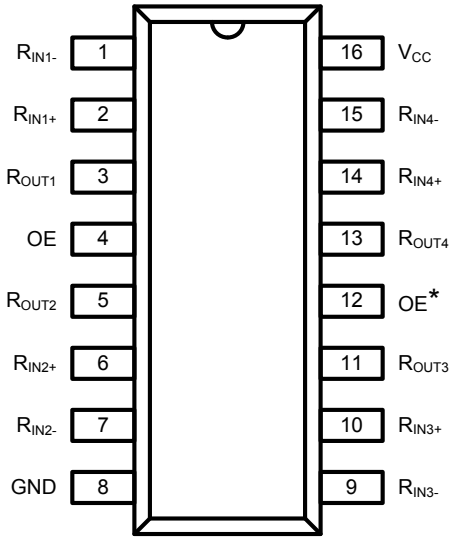
Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF90LVDX032-TBU	SOIC-16(N)	Tube / 48	TF YYWW TFX032TB Lot ID
TF90LVDX032-TBG	SOIC-16(N)	T&R / 500	
TF90LVDX032-6CU	TSSOP-16	Tube / 94	TF YYWW TFX0326C Lot ID
TF90LVDX032-6CG	TSSOP-16	T&R / 1000	

Replace X with S for No Termination, or T for Termination.

Pin Diagram



SOIC-16 or TSSOP-16

Logic Table

OE	OE*	$R_{IN+} - R_{IN-}$	R_{OUT}
Any other combination		≥ 100 mV	H
		≤ -100 mV	L
		Failsafe condition	H
0	1	Don't Care	Disabled

Table 1. Output Enables Truth Table

Pin Descriptions

PIN NAME	PIN NUMBER	PIN TYPE	PIN DESCRIPTION
R_{IN1+}, R_{IN1-}, R_{IN2+}, R_{IN2-}, R_{IN3+}, R_{IN3-}, R_{IN4+}, R_{IN4-}	2, 1, 6, 7, 10, 9, 14, 15	LVDS inputs	Non-inverting and inverting LVDS receiver input pins.
R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}	3, 5, 11, 13	LVCMOS outputs	Receiver LVCMOS output pins.
OE, OE*	4, 12	LVCMOS inputs	Receiver output enable pins. When OE is high or OE* is low or open, the receiver outputs are enabled. When OE is low and OE* is high, the receiver outputs are disabled.
V_{CC}	16	Power	Power supply pin. Bypass V_{CC} to GND with 0.1 µF and 0.01 µF ceramic capacitors.
GND	8	Power	Ground or circuit common pin.

Absolute Maximum Ratings[1]

V_{CC} to GND.....-0.3V to +4V
Inputs
OE, OE* to GND.....-0.3V to V_{CC} + 0.3V
R_{IN+}, R_{IN-} to GND..... -8.0V to +13.0V
V_{ID} (R_{IN}+ to R_{IN}-).....-6V to +6V (LVDT -2V to +2V)
Outputs
R_{OUT} to GND.....-0.3V to V_{CC} + 0.3V

Maximum Package Power Dissipation (T_A = +25 °C)
SOIC-16 (derate 13.8 mW/°C above +25 °C).....1.7 W
TSSOP-16 (derate 9.7 mW/°C above +25 °C).....1.2W

SOIC-16 Thermal Resistance
θ_{JC}.....41 °C/W
θ_{JA}.....72 °C/W

TSSOP-16 Thermal Resistance
θ_{JC}.....29 °C/W
θ_{JA}.....103 °C/W

Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 4s) .....+260°C

ESD Ratings
HBM[1].....8 kV
MM[2].....250 V

1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1 Human Body Model, applicable standard JESD22-A114-C
2 Machine Model, applicable standard JESD22-A115-A

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply Voltage	V_{CC}	3	3.3	3.6	V
V_{IH}	High-level input voltage	OE, OE*	2		V_{CC}	V
V_{IL}	Low-level input voltage	OE, OE*	0		0.8	V
V_{ID}	Differential input voltage	R_{IN+}, R_{IN-}	0.1	0.35	1	V
V_{IN}	Input voltage	R_{IN+}, R_{IN-}	-7		12	V
T_A	Operating free-air temperature	All	-40	25	85	°C

Electrical Characteristics

Over recommended operating conditions ***(NOTE1)***, unless otherwise specified. Typical values are V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter		Conditions	MIN	TYP	MAX	Unit
LVCMOS Input Specifications (OE, OE* pins)							
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			GND		0.8	V
I_{IH}	High-level input current		V_{CC} = 3.6V V_{IN} = 3.6V	-10	0	10	µA
I_{IL}	Low-level input current		V_{CC} = 0 or 3.6V V_{IN} = 0V	-10	0	10	µA
V_{CL}	Input clamp voltage ***(NOTE2)***		I_{CL} = -18 mA, V_{CC} = 0V	-1.5	-0.9		V
LVCMOS Output Specifications (R_{OUT} pins)							
V_{OH}	Output high voltage		I_{OH} = -0.4 mA, V_{ID} = 200 mV	2.7	3.2		V
			I_{OH} = -0.4 mA, input open	2.7	3.2		V
V_{OL}	Output low voltage		I_{OL} = 2 mA, V_{ID} = -200 mV		0.05	0.25	V
I_{OS}	Output short circuit current ***(NOTE1), (NOTE3)***		Enabled, V_{OUT} = 0V		-50	-100	mA
I_{OZ}	Output High-Z current		Disabled, V_{OUT} = 0V or V_{CC}	-10		10	µA
LVDS Input Specifications (R_{IN+}, R_{IN-} pins)							
V_{TH}	Differential input high threshold		V_{ICM} = -7.0V to 12.0V ***(NOTE4)***		0	100	mV
V_{TL}	Differential input low threshold			-100	0		mV
V_{ID}	Differential input voltage			0.1	0.35	1	V
V_{ICM}	Input common mode voltage		V_{ID} = 100 mV	-7.0		12.0	V
I_{IN}	Input current V_{CC} = 0 or 3.6V	TF90LVDS032	0V≤V_{IN+}≤2.4V, V_{IN-}=1.2V	-15		10	µA
			-4V≤V_{IN+}≤6.4V, V_{IN-}=open	-50		50	µA
			-7V≤V_{IN+}≤12V, V_{IN-}=open	-85		130	µA
		TF90LVDT032	0V≤V_{IN+}≤2.4V, V_{IN-}=open	-30		20	µA
			-4V≤V_{IN+}≤6.4V, V_{IN-}=open	-100		100	µA
			-7V≤V_{IN+}≤12V, V_{IN-}=open	-140		185	µA
C_{IN}	Input capacitance		R_{IN+} or R_{IN-} to GND		4		pF
R_{IN}	Input termination resistor		TF90LVDT032 only		100		Ω
Power Supply Current Specifications							
I_{CC}	Power supply current		OE = 1 or OE* = 0 Not switching		5	7	mA
I_{CCZ}	Power supply current with disabled outputs		OE = 0 and OE* = 1		1	2	mA

NOTE1 *Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.*

NOTE2 *This specification is not production tested and is guaranteed by design simulations.*

NOTE3 *Output short circuit current (I_{OS}) is specified as magnitude only. The minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification. Specified for momentary short condition durations only.*

NOTE4 *Recommended operating conditions for the R_{in+} and R_{in-} pins is over the range of -7.0V to 12.0V. Therefore, caution should be taken not to exceed these values or the maximum Differential Input voltage of 1.0V.*

Switching Characteristics

Over recommended operating conditions, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications *(NOTES 5, 6 and 7)*						
t_{PLH}	Propagation delay, low-to-high	Figures 1 and 2 C_L=15pF V_{ID}=200mV V_{ICM} = 1.2V ***(NOTE12)***	1.3	2.1	3.3	ns
t_{PHL}	Propagation delay, high-to-low		1.3	2.1	3.3	ns
t_r	Rise time			0.35	1	ns
t_f	Fall time			0.3	1	ns
$t_{SK(p)}$	Pulse skew ***(NOTE 8)***			50	300	ps
$t_{SK(c-c)}$	Channel-to-channel skew ***(NOTE9)***			100	400	ps
$t_{SK(p-p)}$	Part-to-part skew ***(NOTE10)***				1.5	ns
t_{PLZ}	Disable time, low-to-high Z	Figures 3 and 4 R_L = 2KΩ C_L=15pF V_{ID}=200mV V_{ICM} = 1.2V ***(NOTE12)***		8	14	ns
t_{PHZ}	Disable time, high-to-high Z			8	14	ns
t_{PZL}	Enable time, high Z-to-low			8	14	ns
t_{PZH}	Enable time, high Z-to-high			8	14	ns
f_{MAX}	Maximum operating frequency ***(NOTES 11 and 12)***	Figure 1 C_L=15pF		200		MHz

NOTE5 *Generator output characteristics (unless otherwise specified): f = 1 MHz, Z_0 = 50Ω, t_r < 1 ns, t_f < 1 ns .*

NOTE6 *All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.*

NOTE7 *Switching Characteristic specifications are not production tested and are guaranteed by statistical analysis of characterization data.*

NOTE8 *$t_{SK(p)}$, pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).*

NOTE9 *$t_{SK(c-c)}$, channel-to-channel skew, is the difference in propagation delay time between channels on the same device at any operating temperature and supply voltage.*

NOTE10 *$t_{SK(p-p)}$ part-to-part skew, is the difference in propagation delay time between devices operating at the same power supply voltage and within 5 °C of each other within the operating temperature range.*

NOTE11 *Generator output characteristics for the f_{MAX}: Z_0 = 50Ω, $t_r = t_f$ < 1 ns, 50% duty cycle, 1.05V to 1.35V peak to peak. Output Criteria: 60%/40% duty cycle, VOL (max 0.4V), VOH (min 2.7V) .*

NOTE12 *The capacitive load C_L includes test fixture, probe and lumped capacitance.*

Test Circuits and Timing Diagrams

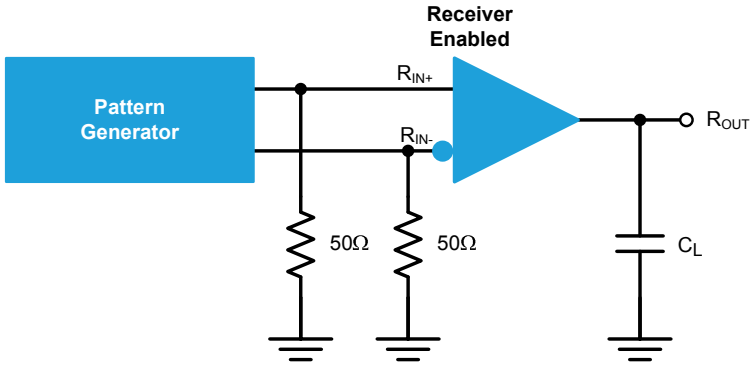


Figure 1. Receiver Propagation Delay and Transition Time Test Setup

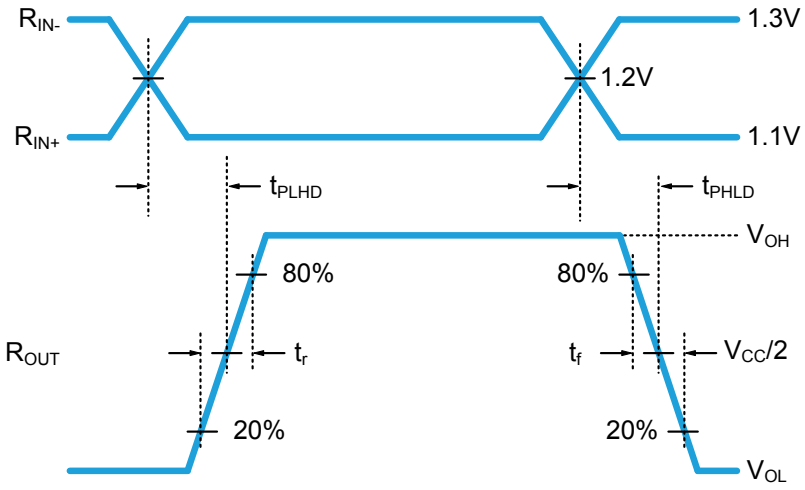


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams

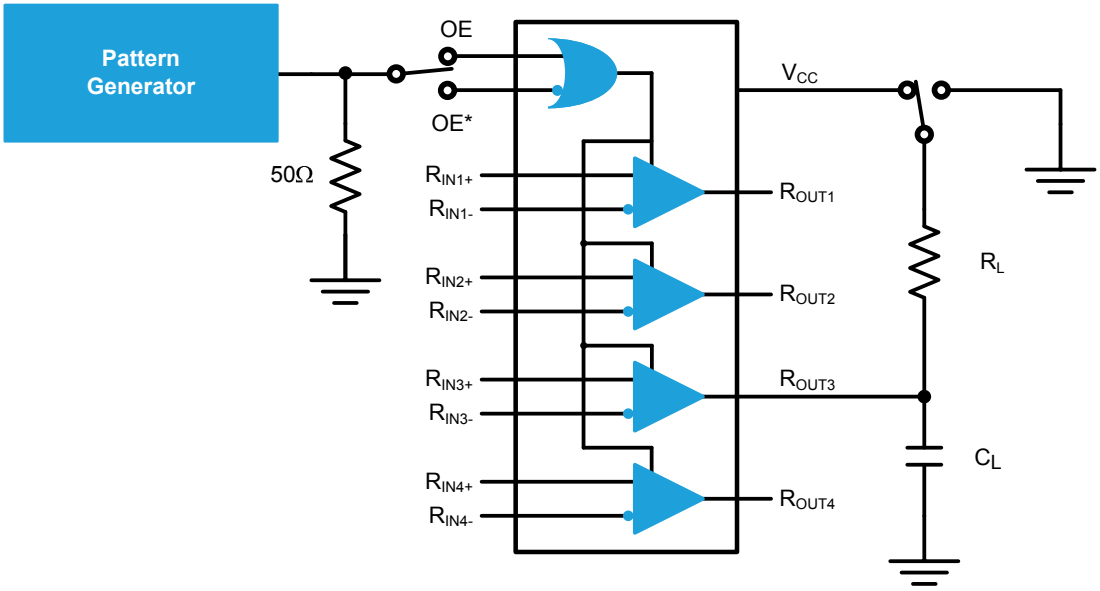


Figure 3. Receiver High-Z Delay Test Setup

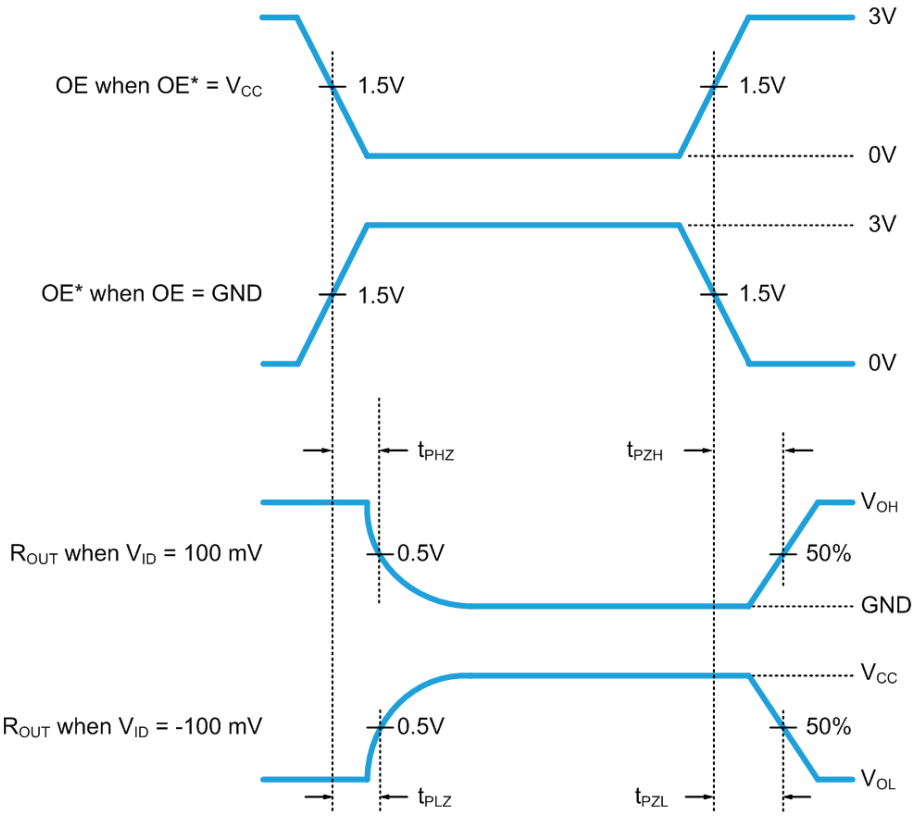
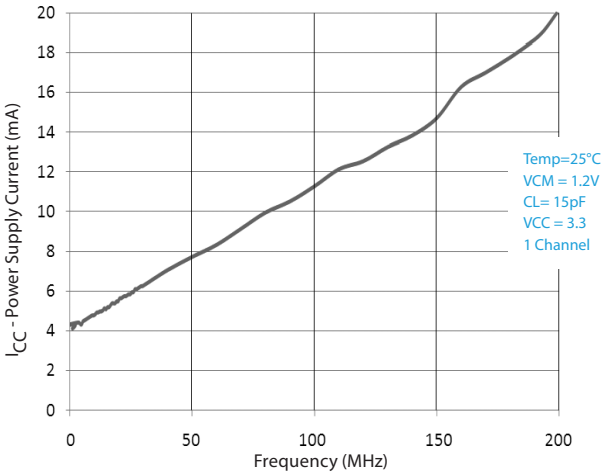


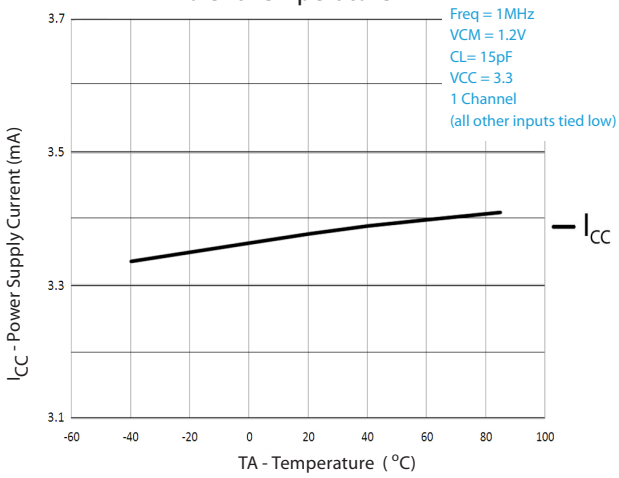
Figure 4. Receiver High-Z Delay Waveforms

Typical Performance Curves

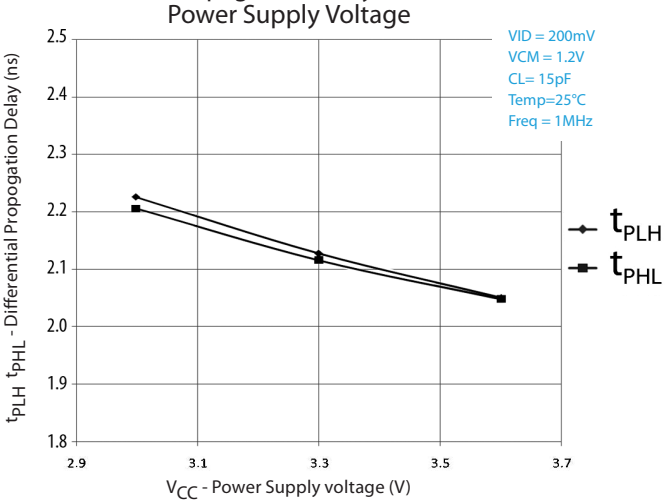
Power Supply Current vs Frequency



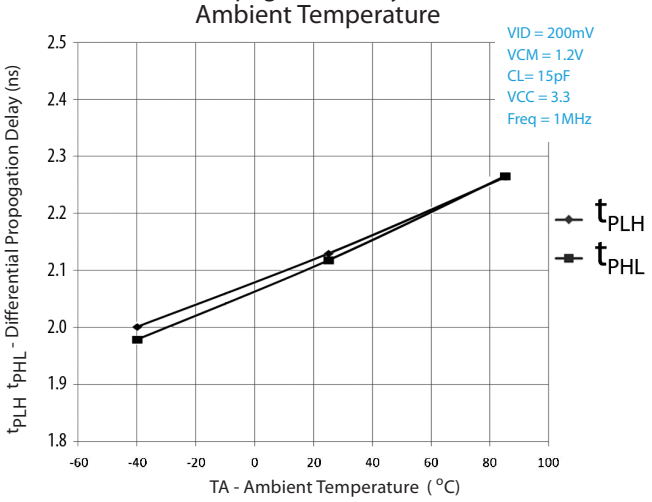
Power Supply Current vs Ambient Temperature



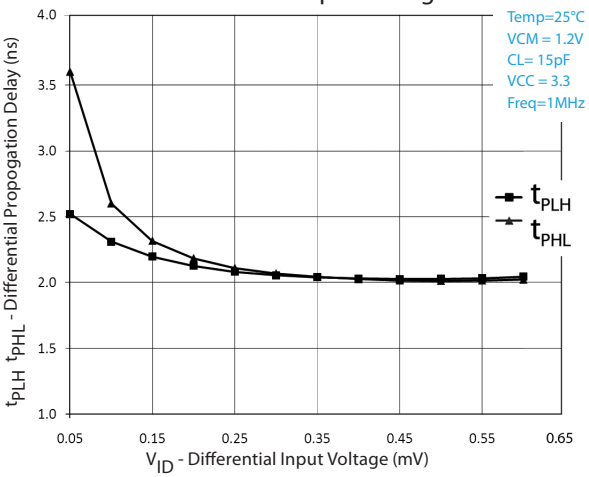
Propagation Delay vs Power Supply Voltage



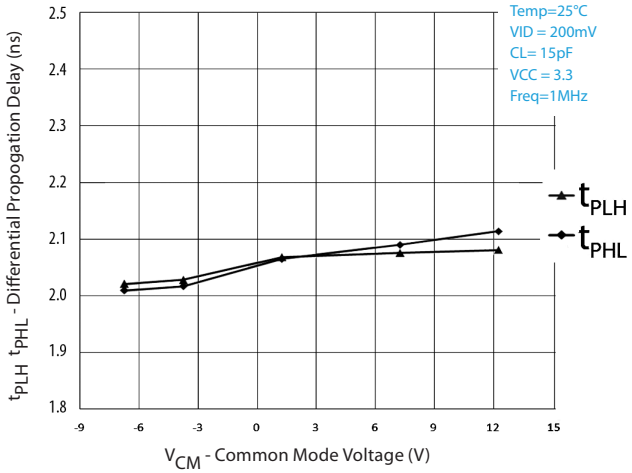
Propagation Delay vs Ambient Temperature



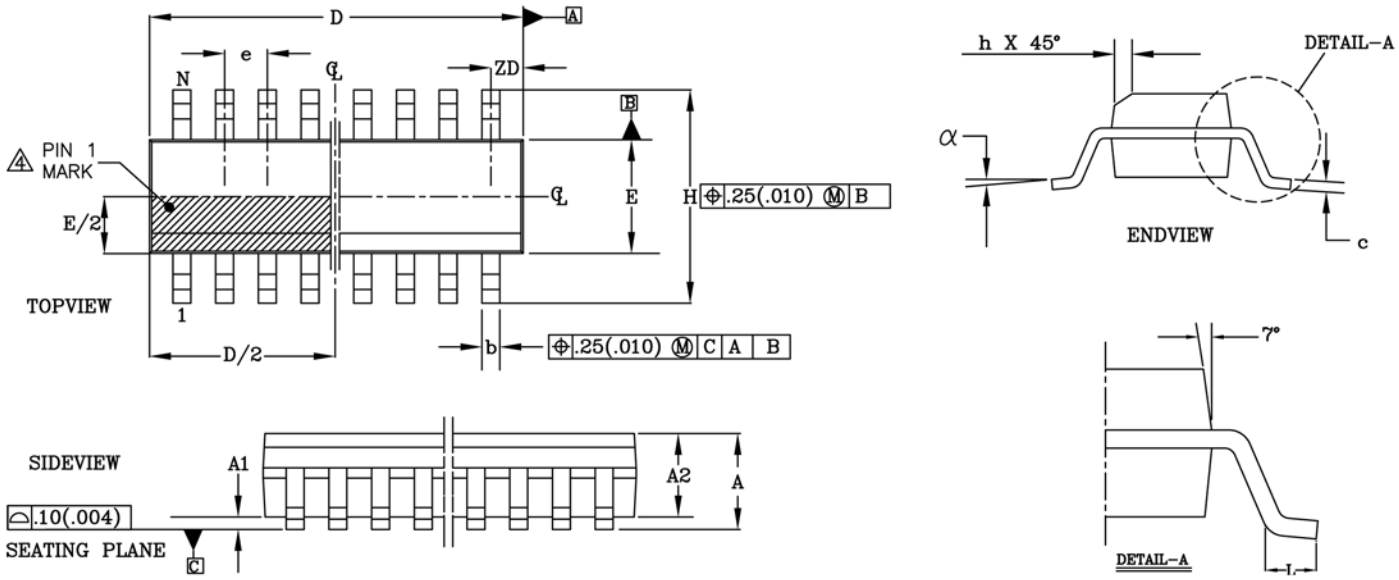
Propagation Delay vs Differential Input Voltage



Propagation Delay vs Common Mode Voltage



Package Dimensions (SOIC-16)



SYMBOL	SOIC–16LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51 REF	
A2	1.37	1.57

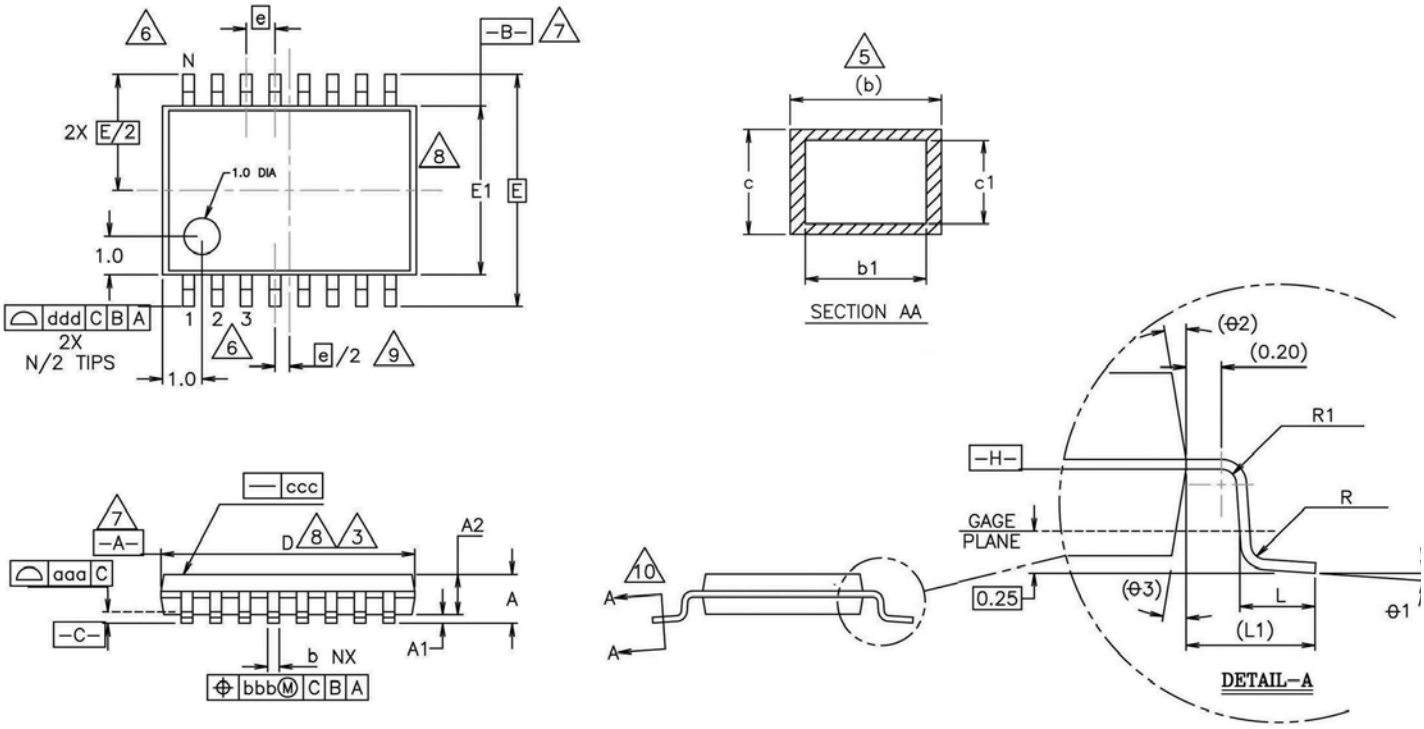
SYMBOL	SOIC–16LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

4. DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

Package Dimensions (TSSOP-16 Please contact support@telekenfunsemi.com for availability)



	0.65mm LEAD PITCH			NOTE
	MIN	NOM	MAX	
A	---	---	1.10	---
A1	0.05	---	0.15	---
A2	0.85	0.90	0.95	---
L	0.50	0.60	0.75	---
R	0.09	---	---	---
R1	0.09	---	---	---
b	0.19	---	0.30	*5*
b1	0.19	0.22	0.25	---
c	0.09	---	0.20	---
c1	0.09	---	0.16	---
θ1	0°	---	8°	---
L1	1.0 REF			---
aaa	0.10			---
bbb	0.10			---
ccc	0.05			---
ddd	0.20			---
e	0.65 BSC			---
θ2	12° REF			---
θ3	12° REF			---
NOTE	*1,2*			

D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	16		

NOTES:

1 ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2 DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3 DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5 DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM FOR 0.5 MM PITCH PACKAGES.

6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7 DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

8 DIMENSIONS 'D' AND 'E1' ARE TO BE DETERMINED AT DATUM PLANE –H–.

9 THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE. FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE, DATUM A.

10 CROSS SECTION A–A TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEADTIP.

11 THIS VARIATION IS NOT REGISTERED WITH JEDEC.

12 PACKAGE SURFACE FINISHING:
(I) TOP: MATTE (CHARMILLES: #18~30)
(II) BOTTOM: MATTE (CHARMILLES: #12~27)

Notes

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