TELEFUNKEN
Semiconductors

TF90LVDS031

Quad LVDS Line Driver

Features

- **DC to 400 Mbps / 200 MHz low noise, low skew, low power operation**
  - **—300 ps (max) channel-to-channel skew**
  - **—250 ps (max) pulse skew**
  - **—23 mA (max) power supply current**
- **LVDS outputs conform to TIA/EIA-644-A standard**
- **Standard output enable scheme eliminates power consumption when device is not in use**
- **Guaranteed operation within industrial temperature range-40° to +85°C**
- **Available in space saving SOIC-16 and TSSOP-16 packages**
- **For Point to Point Applications**
- **Pin and function compatible with DS90LV031A and SN65LVDS31**

Description

The TF90LVDS031 is a 400 Mbps Quad LVDS (low voltage differential signaling) Line Driver optimized for high-speed, low power, low noise transmission over controlled impedance (approximately 100Ω) transmission media (e.g. cables, printed circuit board traces, backplanes).

The TF90LVDS031 accepts four LVCMOS / LVTTL signals and translates them to four LVDS signals. Its differential outputs can be disabled and put in a high-impedance state via two enable pins, OE and OE*.

Low 300 ps (max) channel-channel skew and 250 ps (max) pulse skew ensure reliable communication in high-speed links that are highly sensitive to timing error.

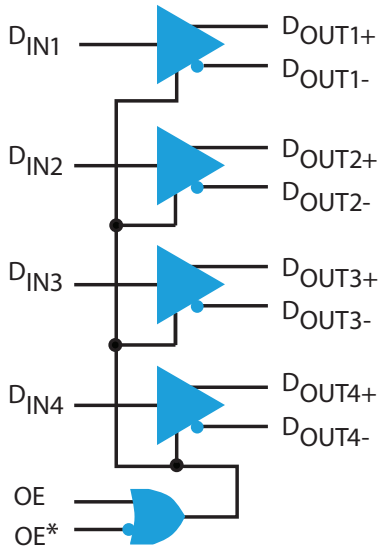
Supply current is 23 mA (max). LVDS outputs conform to the ANSI/EIA/TIA-644-A standard. The TF90LVDS031 is offered in 16-pin SOIC and TSSOP packages and operates over an extended -40 °C to +85 °C temperature range.

Applications

- Digital Copiers
- Wireless Base Stations
- Telecom / Datacom
- Network Routing

SOIC-16(N)   TSSOP-16

Function Diagram

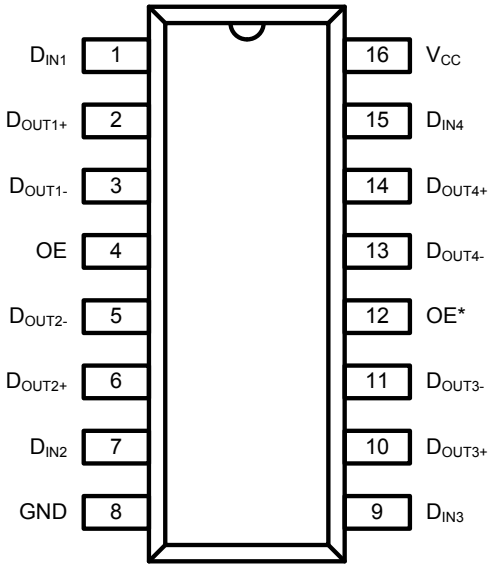


Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF90LVDS031-TBU	SOIC-16(N)	Tube / 48	TF YYWW TFS031TB Lot ID
TF90LVDS031-TBG	SOIC-16(N)	T&R / 500	
TF90LVDS031-6CU	TSSOP-16	Tube / 94	TF YYWW TFS0316C Lot ID
TF90LVDS031-6CG	TSSOP-16	T&R / 1000	

Pin Diagram



SOIC-16 or TSSOP-16

Logic Table

OE	OE*	D_{OUT+}	D_{OUT-}
0	0	Enabled	Enabled
0	1	Disabled	Disabled
1	0	Enabled	Enabled
1	1	Enabled	Enabled

Table 1. Output Enables Truth Table

Pin Descriptions

PIN NAME	PIN NUMBER	PIN TYPE	PIN DESCRIPTION
D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}	1, 7, 9, 15	LVCMOS inputs	Driver LVCMOS input pins.
D_{OUT1}+, D_{OUT1}–, D_{OUT2}+, D_{OUT2}–, D_{OUT3}+, D_{OUT3}–, D_{OUT4}+, D_{OUT4}–,	2, 3, 5, 6, 10, 11, 13, 14,	LVDS outputs	Non-inverting and inverting LVDS output pins.
OE, OE*	4, 12	LVCMOS inputs	Driver output enable pins. When OE is high or OE* is low or open, the driver outputs are enabled. When OE is low and OE* is high, the driver outputs are disabled.
V_{CC}	16	Power	Power supply pin. Bypass V_{CC} to GND with 0.1 µF and 0.01 µF ceramic capacitors.
GND	8	Power	Ground or circuit common pin.

Absolute Maximum Ratings[1]

V_{CC} to GND.....-0.3V to +4V
Inputs
OE, D_{IN} to GND.....-0.3V to V_{CC} + 0.3V
Outputs
D_{OUT+}, D_{OUT-} to GND.....-0.3V to V_{CC} + 0.3V

Maximum Package Power Dissipation (T_A = +25 °C)
SOIC-16 (derate 13.8 mW/°C above +25 °C).....1.7 W
TSSOP-16 (derate 9.7 mW/°C above +25 °C).....1.2 W

SOIC-16 Thermal Resistance
θ_{JC}.....41 °C/W
θ_{JA}.....72 °C/W

TSSOP-16 Thermal Resistance
θ_{JC}.....29 °C/W
θ_{JA}.....103 °C/W

Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Lead Temperature (soldering, 4s) .....+260°C

ESD Ratings
HBM[1].....8 kV
MM[2].....250V
CDM[3].....1.25 kV

1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1 Human Body Model, applicable standard JESD22-A114-C
2 Machine Model, applicable standard JESD22-A115-A
3 Field Induced Charge Device Model, applicable standard JESD22-C101-C

Recommended Operating Conditions

Symbol	Parameter	Pins	MIN	TYP	MAX	Unit
V_{CC}	Supply Voltage	V_{CC}	3	3.3	3.6	V
V_{IH}	High-level input voltage	OE, OE*, D_{IN}	2		V_{CC}	V
V_{IL}	Low-level input voltage	OE, OE*, D_{IN}	0		0.8	V
T_A	Operating free-air temperature	All	-40	25	85	°C

Electrical Characteristics

Over recommended operating conditions ***(NOTE1)***, unless otherwise specified. Typical values are V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVCMOS Specifications (OE, OE*, D_{IN} pins)						
V_{IH}	High-level input voltage		2.0		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.8	V
I_{IH}	High-level input current	V_{CC} = 3.6V V_{IN} = 3.6V	-10		10	µA
I_{IL}	Low-level input current	V_{CC} = 3.6V V_{IN} = 0V	-10		10	µA
V_{CL}	Input clamp voltage ***(NOTE2)***	I_{CL} = -18 mA, V_{CC} = 0V	-1.5	-0.9		V
LVDS Output Specifications (D_{OUT+}, D_{OUT-} pins)						
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100Ω Figure 1	250	370	450	mV
$\|\Delta V_{OD}\|$	Change in magnitude of V_{OD} for complimentary output states		-35		35	mV
$V_{OCM(ss)}$	Steady-state output common mode voltage		1.125	1.25	1.375	V
$\Delta V_{OCM(SS)}$	Change in magnitude of $V_{OCM(ss)}$ for complimentary output states		-25		25	mV
V_{OH}	Output high voltage	R_L = 100Ω Figure 1		1.43	1.6	V
V_{OL}	Output low voltage		0.9	1.06		V
I_{OS}	Output short circuit current ***(NOTE3)***	Enabled, D_{OUT+} or D_{OUT-} = 0V			-13	mA
I_{OSD}	Differential output short circuit current ***(NOTE3)***	Enabled, V_{OD} = 0V			-13	mA
I_{OZ}	High-impedance output current	Disabled, Vout = 0V or Vcc	-14		+14	µA
C_{OUT}	Output capacitance	D_{OUT+} or D_{OUT-} to GND		3		pF
Power Supply Current Specifications						
I_{CC}	Power supply current without output loads	Enabled D_{IN} = 0V or V_{CC}		1	2	mA
I_{CCL}	Power supply current with output loads	Enabled D_{IN} = 0V or V_{CC}, R_L =100Ω		16	23	mA
I_{CCZ}	Power supply current with disabled outputs	Disabled OE = 0 and OE* = 1		1	2	mA

NOTE1 *Current into device pin is defined as positive. Current out of the device is defined as negative. All voltages are referenced to ground, unless otherwise specified.*

NOTE2 *This specification is not production tested and is guaranteed by design simulations.*

NOTE3 *Output short circuit current (I_{OS}) is specified as magnitude only. The minus sign indicates direction only.*

Switching Characteristics

Over recommended operating conditions, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = 25 °C.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
LVDS AC Specifications *(Notes 4, 5 and 6)*						
t_{PLH}	Propagation delay, low-to-high	Figures 2 and 3 R_L = 100Ω C_L=15pF ***(Note 12)***	0.6	1	1.9	ns
t_{PHL}	Propagation delay, high-to-low		0.6	1	1.9	ns
t_r	Rise time			.35	1	ns
t_f	Fall time			.35	1	ns
$t_{SK(p)}$	Pulse skew ***(Note 7)***			50	250	ps
$t_{SK(c-c)}$	Channel-to-channel skew ***(Note 8)***			80	300	ps
$t_{SK(p-p)A}$	Part-to-part skew ***(Note 9)***				1	ns
$t_{SK(p-p)B}$	Part-to-part skew ***(Note 10)***				1.3	ns
t_{PLZ}	Disable time, low-to-high Z	Figures 4 and 5 R_L = 100Ω C_L=15pF ***(Note 12)***			5	ns
t_{PHZ}	Disable time, high-to-high Z				5	ns
t_{PZL}	Enable time, high Z-to-low				5	ns
t_{PZH}	Enable time, high Z-to-high				5	ns
f_{MAX}	Maximum operating frequency ***(Note 11)***	Figure 2	200	250		MHz

NOTE4 *Generator output characteristics (unless otherwise specified): f = 1 MHz, Z_0 = 50Ω, t_r < 1 ns, t_f< 1 ns .*

NOTE5 *All input voltages are for one channel unless otherwise specified. Other inputs are set to GND.*

NOTE6 *Switching Characteristic specification are not production tested and are guaranteed by statistical analysis of characterization data .*

NOTE7 *$t_{SK(p)}$, pulse skew, is the magnitude difference in propagation delay time between the positive going edge and the negative going edge of the same channel ($t_{SK(p)} = |t_{PLH} - t_{PHL}|$).*

NOTE8 *$t_{SK(c-c)}$, channel-to-channel skew, is the difference in propagation delay time between channels on the same device at any operating temperature and supply voltage.*

NOTE9 *$t_{SK(p-p)A}$ part-to-part skew "A", is the difference in propagation delay time between devices operating at the same power supply voltage and within 5 °C of each other within the operating temperature range.*

NOTE10 *$t_{SK(p-p)B}$ part-to-part skew "B", is the difference in propagation delay time between devices operating at any recommended power supply voltage and ambient temperature. It is also defined as |MIN -MAX| propagation delay (t_{PLH} or t_{PHL}).*

NOTE11 *Generator output characteristics for the f_{MAX}: Z_0 = 50Ω, $t_r = t_f$ < 1 ns, 50% duty cycle, 0V to 3V amplitude. Output criteria for f_{MAX}: 45% / 55% duty cycle, $V_{OD} \geq$ 250 mV.*

NOTE12 *The capacitive load C_L includes test fixture, probe and lumped capacitance..*

Test Circuits and Timing Diagrams

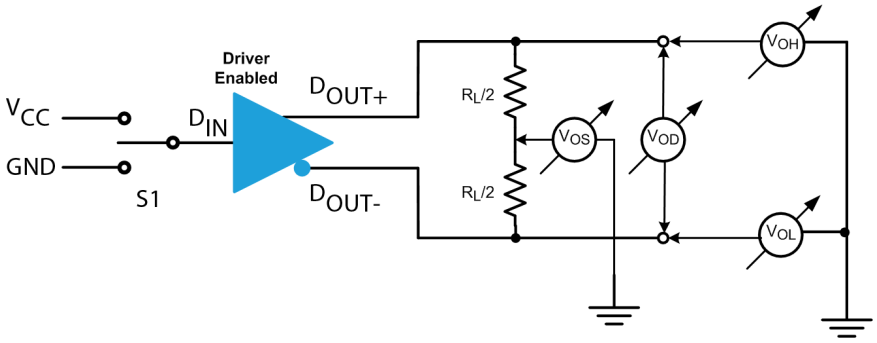


Figure 1. Driver V_{OH} and V_{OL} Test Setup

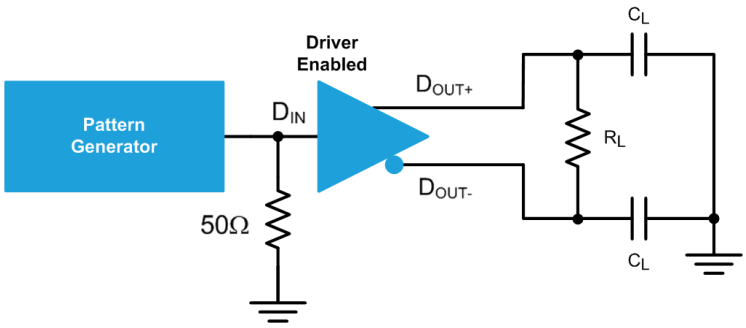


Figure 2. Driver Propagation Delay and Transition Time Test Setup

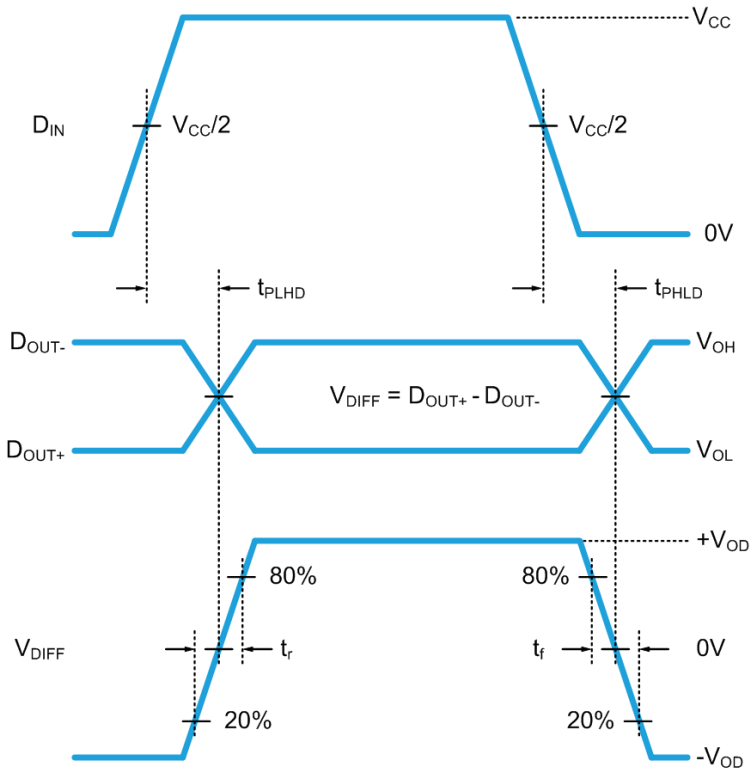


Figure 3. Driver Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams

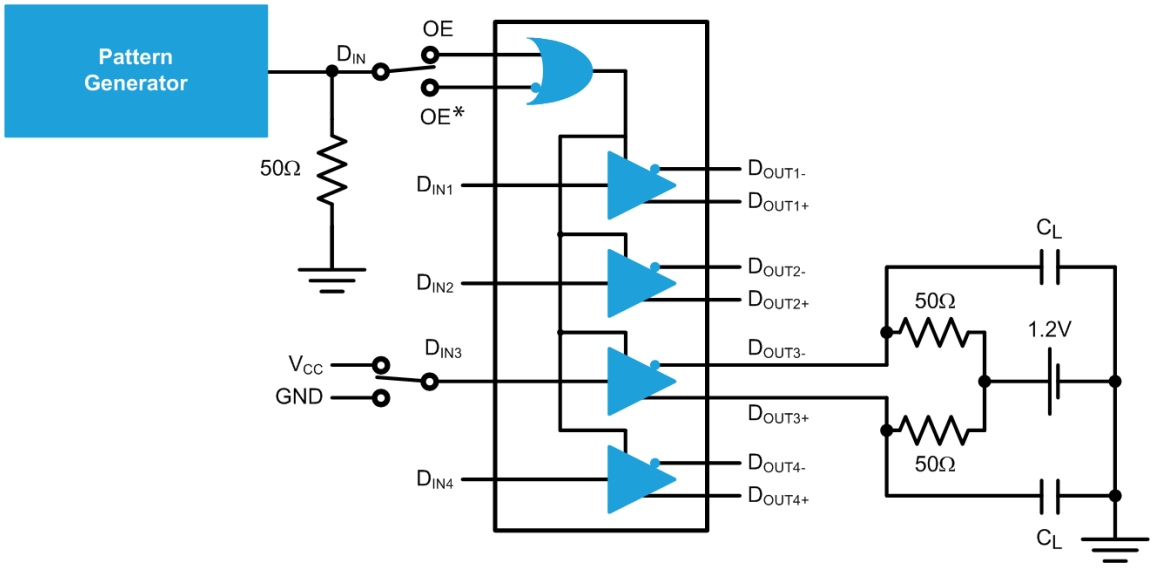


Figure 4. Driver High-Z Delay Test Setup

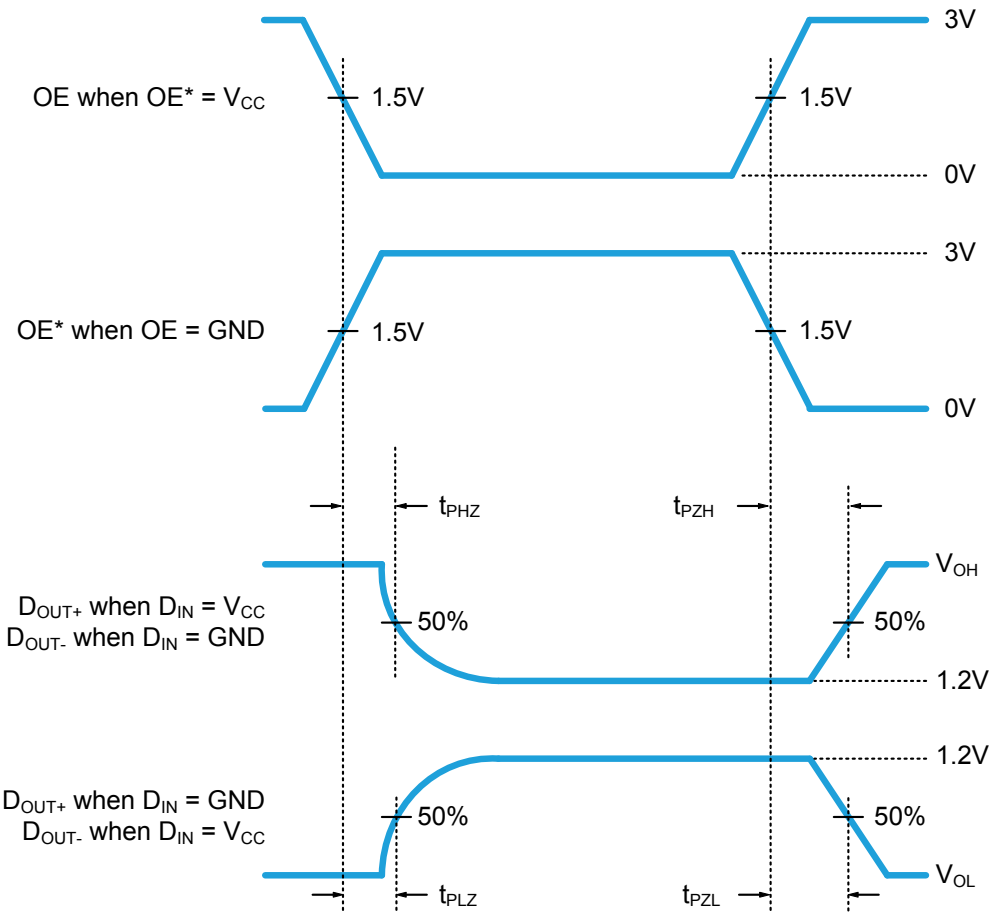
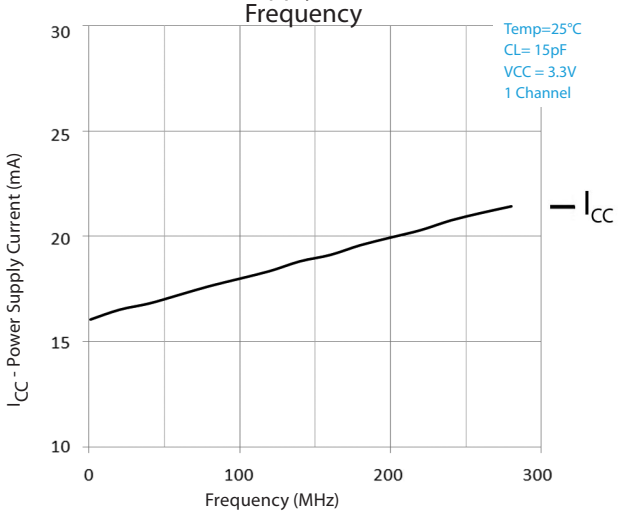


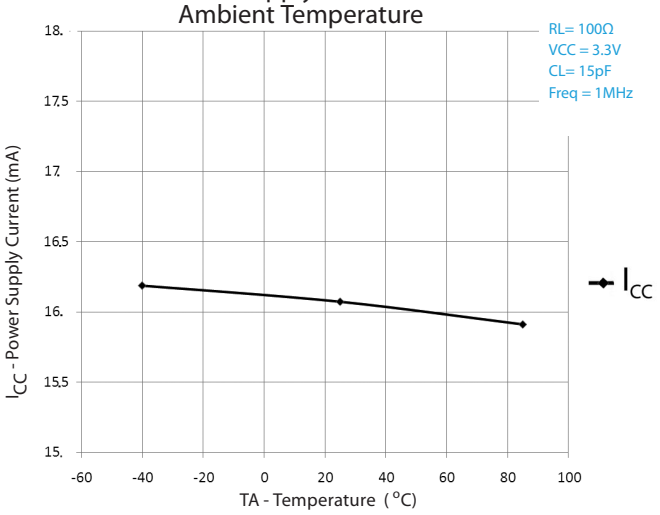
Figure 5. Driver High-Z Delay Waveforms

Typical Performance Curves

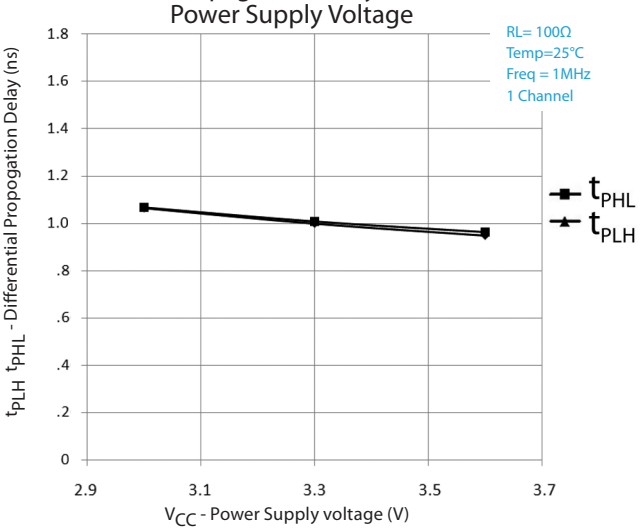
Power Supply Current vs Frequency



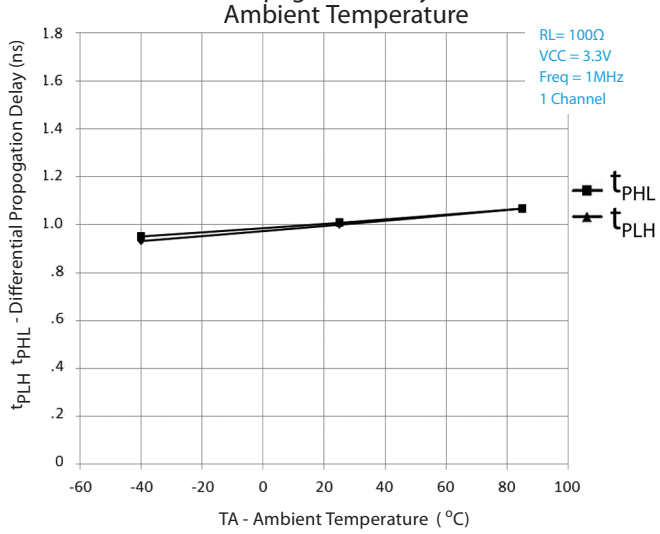
Power Supply Current vs Ambient Temperature



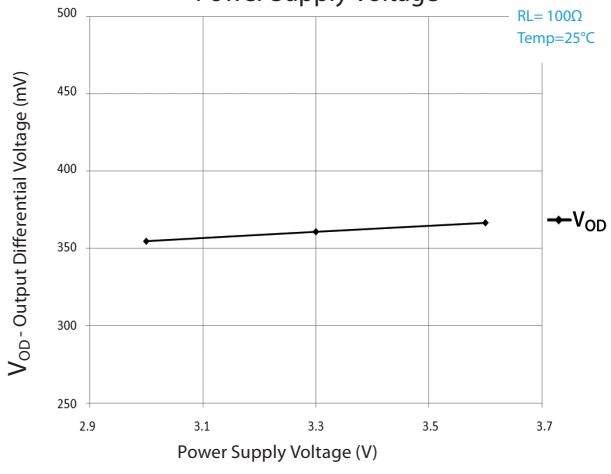
Propagation Delay vs Power Supply Voltage



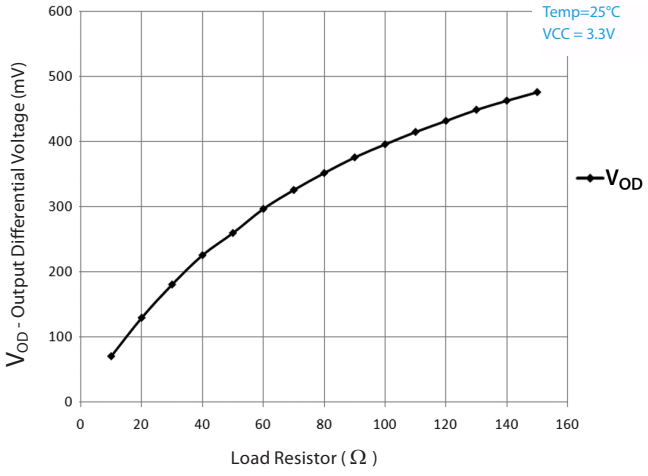
Propagation Delay vs Ambient Temperature



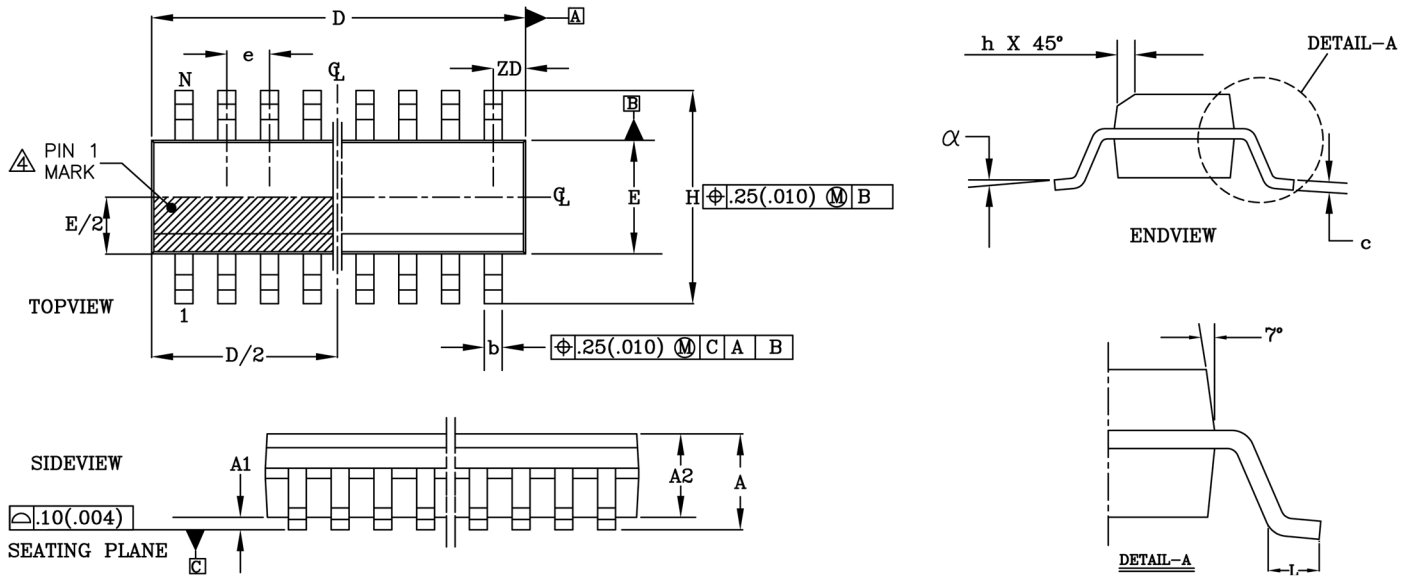
Output Differential Voltage vs Power Supply Voltage



Output Differential Voltage vs Load Resistor



Package Dimensions (SOIC-16)



SYMBOL	SOIC–16LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	9.80	9.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.51 REF	
A2	1.37	1.57

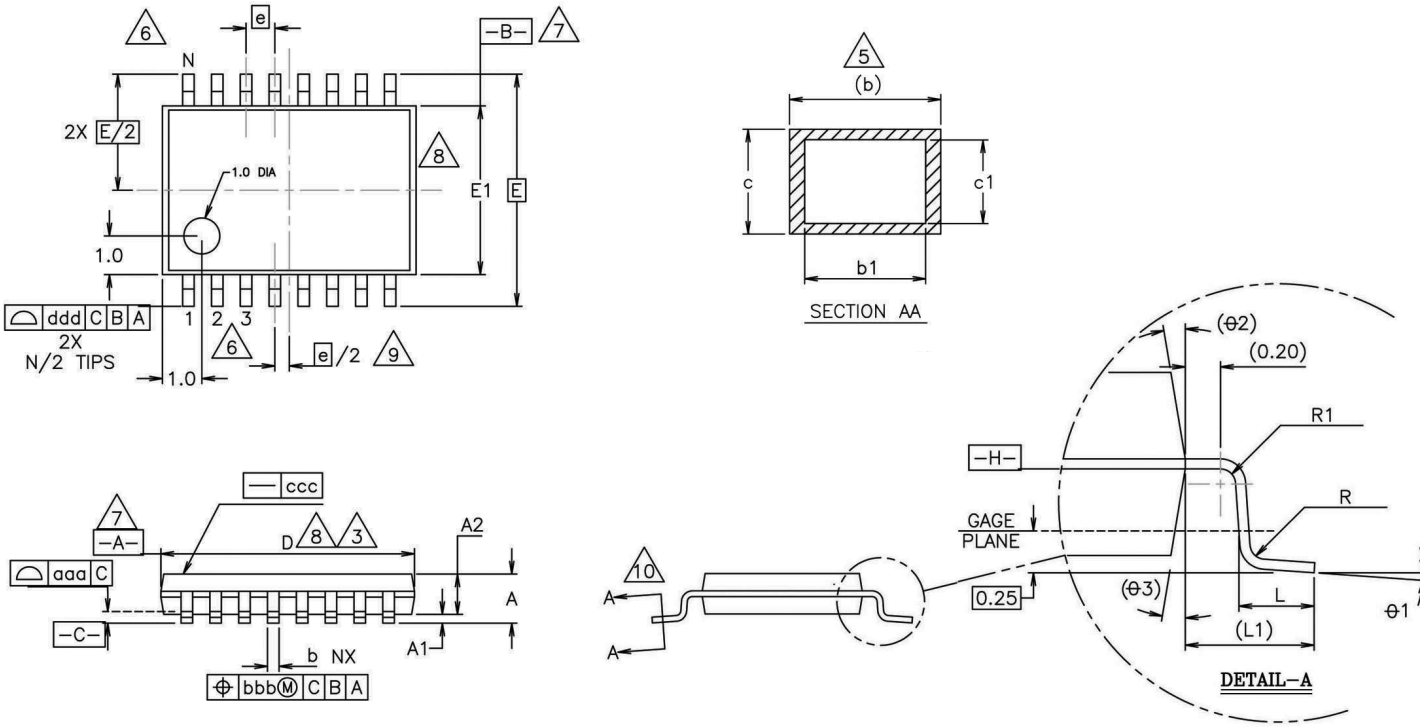
SYMBOL	SOIC–16LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.386	.393
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.020 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

⚠4 DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

Package Dimensions (TSSOP-16 Please contact support@telekenfunsemi.com for availability)



	0.65mm LEAD PITCH			NOTE
	MIN	NOM	MAX	
A	---	---	1.10	---
A1	0.05	---	0.15	---
A2	0.85	0.90	0.95	---
L	0.50	0.60	0.75	---
R	0.09	---	---	---
R1	0.09	---	---	---
b	0.19	---	0.30	*5*
b1	0.19	0.22	0.25	---
c	0.09	---	0.20	---
c1	0.09	---	0.16	---
θ1	0°	---	8°	---
L1	1.0 REF			---
aaa	0.10			---
bbb	0.10			---
ccc	0.05			---
ddd	0.20			---
e	0.65 BSC			---
θ2	12° REF			---
θ3	12° REF			---
NOTE	*1,2*			

D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	16		

NOTES:

1 ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2 DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3 DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5 DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM FOR 0.5 MM PITCH PACKAGES.

6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

7 DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−

8 DIMENSIONS 'D' AND 'E1' ARE TO BE DETERMINED AT DATUM PLANE −H−.

9 THIS DIMENSION APPLIES ONLY TO VARIATIONS WITH AN EVEN NUMBER OF LEADS PER SIDE. FOR VARIATION WITH AN ODD NUMBER OF LEADS PER SIDE, THE "CENTER" LEAD MUST BE COINCIDENT WITH THE PACKAGE CENTERLINE, DATUM A.

10 CROSS SECTION A−A TO BE DETERMINED AT 0.10 TO 0.25 MM FROM THE LEADTIP.

11 THIS VARIATION IS NOT REGISTERED WITH JEDEC.

12 PACKAGE SURFACE FINISHING:
(I) TOP: MATTE (CHARMILLES: #18~30)
(II) BOTTOM: MATTE (CHARMILLES: #12~27)

Notes

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