Telefunken Extended Common Mode LVDS

TELEFUNKEN Semiconductors

APPLICATION NOTE 100
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… how to provide high-speed, robust communication in noisy environments (and avoid RS-485/422).

Telefunken recently introduced LVDS devices that are pin and function compatible with the industry standard but offer a vastly increased common mode that equals the RS-485/422 specification. The new devices provide excellent LVDS speed and power performance with RS-485 noise immunity.

LVDS

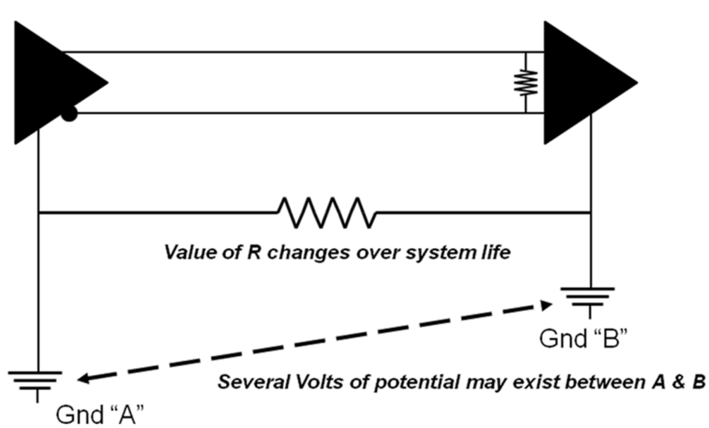
High speed communication links use differential signaling for reasons of bandwidth and power consumption. Due to an outstanding bandwidth to power ratio the dominant differential technology is LVDS. Combining miniscule power consumption and low EMI with high bandwidth, LVDS is used extensively for FPGA and ASIC I/O, video transmission, clock distribution and a variety of other signaling tasks. Pervasive LVDS provides excellent value when bandwidth is compared to either cost or power consumption and since LVDS is so prevalent as an FPGA I/O this is the preferred technology when sending video or sensor data to a central FPGA for routing or processing.

Common Mode

Although LVDS offers an excellent bandwidth to power ratio, the technology has one weakness, that being a relatively narrow common mode. Common Mode refers to the input voltage range with guaranteed operation when the LVDS transmitter and receiver are referenced to different ground planes. The LVDS specification ensures fault free operation when the receiver input signal is between 0 and 2.4 Volts. Since the LVDS transmitter signal is centered at 1.2V and is typically about 400mV, this results in a common mode noise margin of +/- 1 Volt. The 1 Volt of common mode noise margin must account for both instantaneous and steady-state differences between ground potential. Noise margin of 1 Volt of is generally sufficient; however this may create problems in noisy environments.

Ground Bounce and Drift

Local ground at the receiver may vary relative to the transmitter instantaneously – known as "ground bounce" or with a steady state potential difference. Ground bounce (or Vcc droop) typically occurs when large switching currents create a local and temporary voltage variation in a ground or power plane. Good board layout, power and ground planes and the use of decoupling capacitors will reduce but not totally eliminate ground bounce. A steady-state potential difference between grounds can occur in physically distributed systems and/or where return current encounters a resistive path. In some cases as hardware ages, connections can become more resistive, increasing the IR drop in the return path and thus increasing the steady-state potential difference. In either of these situations, or where both may be present, the common mode difference between transmitter and receiver may exceed the specification of the devices and result in either bit errors or a broken communication link. Real world examples have been reported in Telecom, Automotive, Avionics and Industrial applications.



AC Coupling

One approach to eliminate common mode concerns is the use of coupling capacitors on both channels of the differential pair. The coupling caps block the DC portion of the signal but are transparent to the signal edges allowing high-speed communication irrespective of common mode. Capacitive coupling is only viable when the transmitted data is DC balanced, meaning the data is coded such that it contains an equal number of ones and zeros. Coded communications standards such as 8b/10b are DC balanced but this is generally not the case for many other signaling requirements such as video, control signals and non-coded data. Coding data for DC balance also invokes a bandwidth penalty; for example in the case of 8b/10b, 20%.

Comparison to RS-485

The mature RS-485/422 standard is generally used in noisy environments where common mode difference is a known problem. RS-485 is a relatively slow, large swing differential standard that guarantees operation over a common mode of from -7 to +12V. In addition to relatively poor bandwidth, power and EMI performance, RS-485 is not available in standard FPGAs or ASIC I/O libraries and therefore often requires translation at both ends of a communication link.

Summary

LVDS dominates high-speed signaling, offering an attractive combination of high speed, low power and very low EMI. The LVDS standard specifies a 350mV signal swing centered at 1.2V and a common mode of between 0 and 2.4 Volts. This provides 1V of noise margin at both Vcc and Ground and thus the system is guaranteed to operate provided there are never any local Vcc or Ground variations that exceed 1V. For on-card and inside-the-box communication 1 volt of noise margin is generally sufficient provided good layout and decoupling practices are followed. However, for distributed systems or box-to-box communication, 1 volt of noise margin may not be suitable, particularly over the lifetime of the system.

Common Mode differences have historically been resolved by using slow, noisy and power hungry RS-485, AC coupling or other isolation techniques. Telefunken is now launching an extended common mode version of LVDS that meets the TIA/EIA-644A LVDS standard but also extends the common mode to +12 and -7V, the same requirement as RS-485. Applications that could benefit from the high performance yet low cost and low power of LVDS now have a very robust alternative. The TF90LVDS048 Quad LVDS Receiver is offered in an industry standard package and pinout and is completely compatible with existing LVDS transmitters and receivers.

Important Notice

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